A Novel Power Factor Control Scheme for High-Power GTO Current-Source Converter

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***Abstract*—A novel power factor control scheme for high-power gate-turn-off thyristor current-source converters is proposed in this paper. Using both feedforward and feedback control techniques, the proposed scheme guarantees that the input power factor of the converter can be kept at unity or a maximum achievable value. Another feature of this scheme is parameter insensitive, that is, variations in the line and load impedance or changes in the filter capacitor size will not affect the process of tracking the maximum input power factor. No parameters in the control scheme should be adjusted to accommodate such variations or changes. Simulation and experimental results are provided to verify the operating principle of the scheme.**

***Index Terms*— Gate-turn-off converters, high-power rectifier, input power factor control, pulsewidth modulation techniques.**

I. Introduction

A TYPICAL high-power gate-turn-off (GTO) current-source converter is shown in Fig. 1. The GTO devices are usually connected in series to withstand ac line voltages (typically 2300–6900 V). A three-phase filter capacitor C_s is required to assist GTO commutation and, at the same time, to filter out current harmonics produced by the converter. The inductance L_s represents transformer leakage inductance or line reactors connected between the source and converter.

This converter has the features of robust operation and regeneration capability. However, the use of the filter capacitor C_s makes the input power factor leading. For high-power converters (500 kVA and above), the switching frequency is usually limited to several hundred hertz [1], [4]. The converter operated with this low switching frequency requires a relatively large filter capacitor, typically in a range of 0.2–0.6 per unit (refer to Appendix for definition of the per-unit system used in this paper). Therefore, the leading current produced by the capacitor has an adverse effect on the system input power factor.

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A power factor control scheme for the current-source converter was proposed in [5]. A delay angle α between the converter input voltage V_c and current I_w was introduced to compensate the leading capacitor current such that the input power factor could be unity. To achieve unity power factor control, the delay angle α should satisfy the following equation:

$$\alpha = \sin^{-1} \frac{\omega_s C_s V_s}{M_d I_d} \tag{1}$$

where M_d is modulation index which is defined as

$$M_d = \frac{I_w}{I_d}. \tag{2}$$

This control scheme, however, has two drawbacks. One is parameter dependent. As shown in (1), the calculation of delay angle α is based on capacitor size, source frequency, and voltage. Any variations in these quantities will cause a deviation from the unity power factor operation. Another drawback is that the scheme is valid only when unity power factor is achievable. Under certain operating conditions to be discussed in Section II, a unity power factor operation may not be achievable.

A novel power factor control scheme for a high-power GTO current-source converter is proposed in this paper. Using both feedback and feedforward techniques, the proposed control scheme has the following features.

- It can provide unity input power factor when it is achievable.
- It can produce the highest possible power factor, if unity power factor is unachievable.
- It does not require system parameters.

II. Maximum Achievable Power Factor

A phasor diagram of the converter system without using α control is shown in Fig. 2(a). The fundamental component of converter input current I_w is in phase with its phase voltage V_c. The line current I_s is the sum of the converter current I_w and capacitor current I_c and, therefore, leads the voltage V_s by an angle Φ, producing a leading power factor. The nonunity power factor can be compensated by introducing a delay angle α between I_w and V_c, as shown in Fig. 2(b). The relationship between the delay angle α and average dc voltage V_d can be expressed as

$$V_d = \sqrt{1.5}\sqrt{3} V_s M_d \cos\alpha. \tag{3}$$

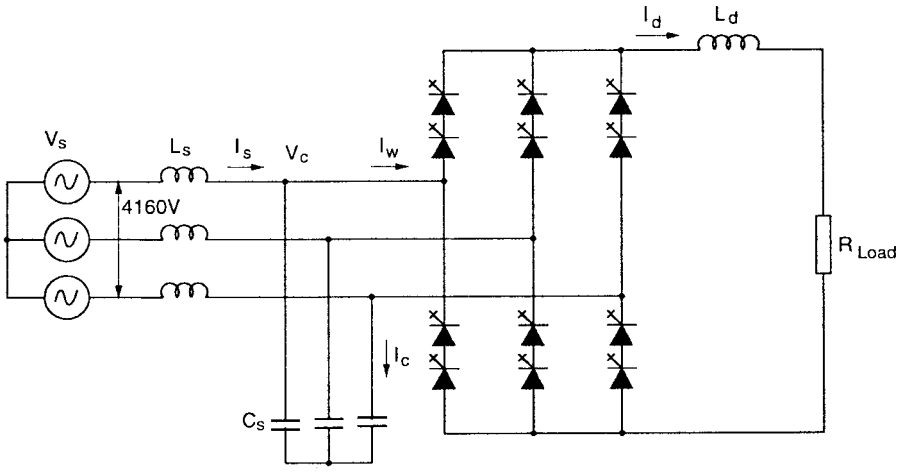

Fig. 1. Circuit diagram of a high-power GTO pulsewidth modulation (PWM) current-source converter.

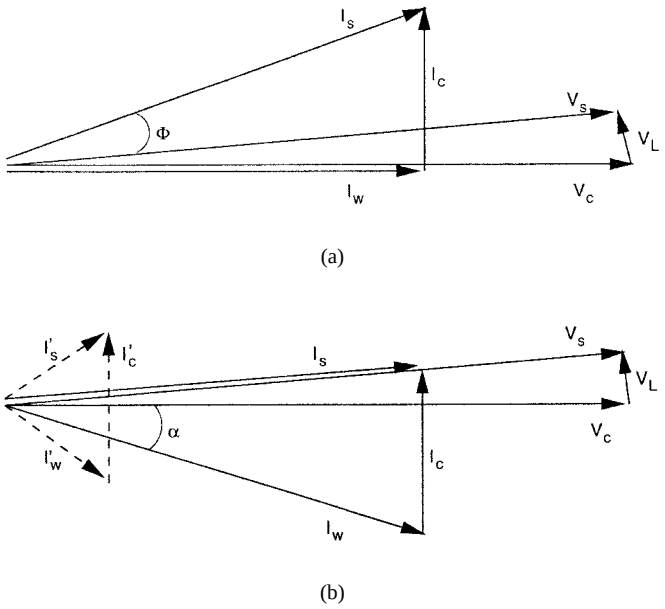

Fig. 2. Phasor diagram of converter system: (a) modulation index control only and (b) power factor control.

In general, a unity power factor can be achieved by increasing the delay angle α and, at the same time, increasing the modulation index M_d to compensate the voltage reduction due to the α increase. This control scheme, however, is not valid under the following operating conditions.

- The converter current I_w is small. Under a light load condition, the converter current I_w at the maximum modulation index is still low, which cannot provide enough lagging component to compensate the leading capacitor current, as shown in Fig. 2(b) with dotted lines. In this case, (1) does not have a solution, since the term $(\omega_s C_s V_s)/(M_d I_d)$ will be greater than one.
- The average dc voltage V_d is close to its rated value. Under this condition, the delay angle α in (3) does not have much room to be adjusted for power factor compensation.

Let us now discuss the operating principle of the proposed scheme. The focus will be placed on how to obtain maximum

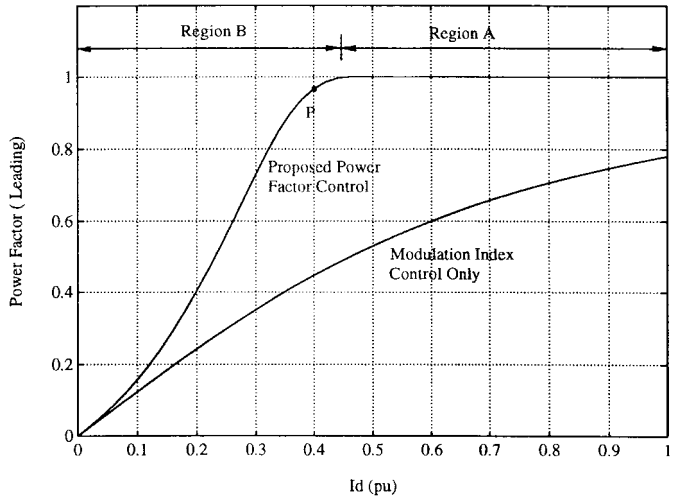

Fig. 3. Power factor versus dc current I_d with $V_d = 0.5$ pu and $C_s = 0.4$ pu.

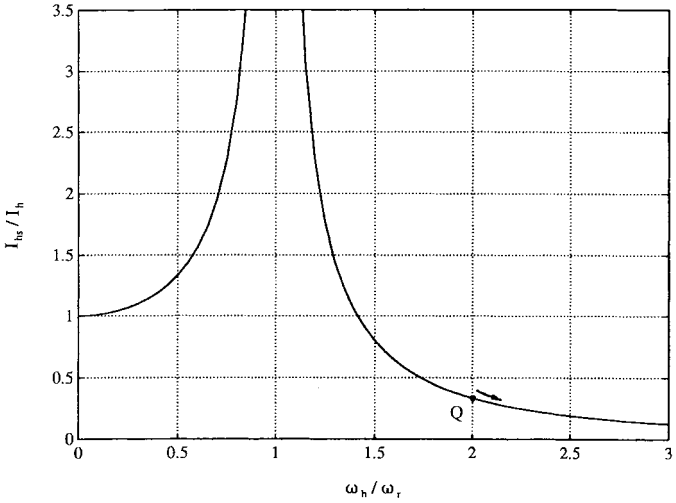

Fig. 4. Relationship between I_{hs}/I_h and ω_h/ω_r.

power factor when a unity power factor is not achievable. The maximum power factor can be obtained by increasing the converter current I_w to its maximum value and, at the same

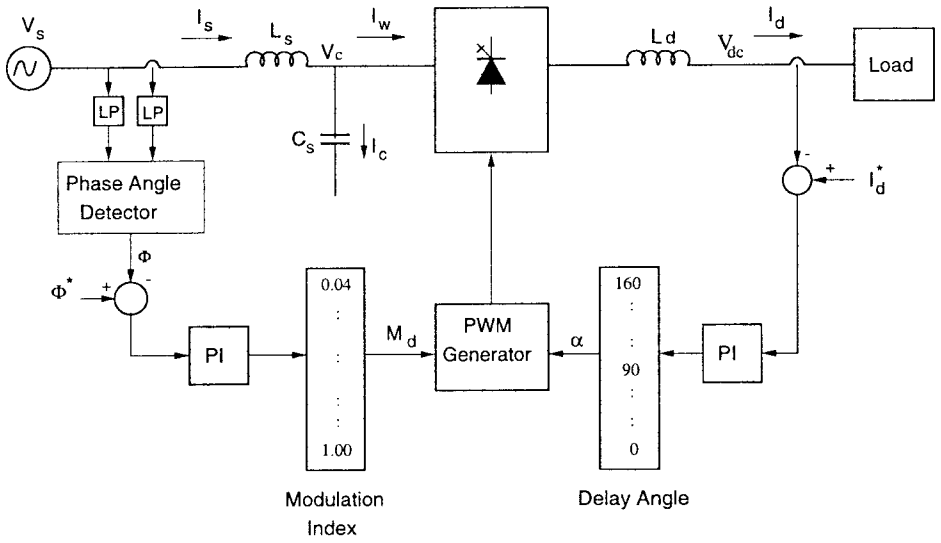

Fig. 5. Proposed power factor control scheme.

TABLE I
SWITCHING PATTERN A AND B

Switching Pattern	A	B
Switching Frequency	360	600
Harmonics Eliminated	5, 7	5,7,11,13
Frequency of Lowest-order Harmonic	11	17
Maximum amplitude of lowest-order harmonic I_h (Worst case)	57%	61%

time, increasing the delay angle α to its highest possible value, such that the angle Φ between source voltage and current is minimized. The maximum I_w can be realized by setting M_d to its maximum value, whereas the highest possible value for the delay angle α is governed by (3) for a given dc voltage.

An example of a power factor profile produced by the proposed scheme is shown in Fig. 3, where it is assumed that the dc voltage is at 50% of its maximum value and the filter capacitor C_s is equal to 0.4 per unit. In region *A*, where the unity power factor is achievable, the power factor is kept at unity, while in region *B*, in which the unity power factor is unachievable due to the lower dc current, the power factor is kept at the highest possible value. Compared with the scheme using modulation index control alone, the proposed scheme can significantly improve the converter input power factor.

III. MINIMUM CAPACITOR SIZE

It is obvious that region *B* decreases with the decrease of capacitor size. As a result, the power factor of the system is improved. However, reducing the capacitor size will increase the system resonant frequency, defined by

$$\omega_r = \frac{1}{\sqrt{L_s C_s}} \text{ pu.} \tag{4}$$

When the resonant frequency approaches the frequency of the lowest order harmonic current I_h generated by the converter, the system will operate in a resonance mode, which should be avoided.

Two switching patterns suitable for high-power converters are listed in Table I, where it is indicated that the maximum amplitude of the lowest order harmonic current I_h is 57% for switching pattern *A* and 61% for pattern *B* [4]. The resonant frequency should be selected such that the amplitude of the harmonic current I_{hs} in the inductor L_s should be much lower than that generated by the converter. The relationship between I_{hs}/I_h and ω_h/ω_r can be described by

$$\frac{I_{hs}}{I_h} = \left| \frac{1}{1 - \left(\frac{\omega_h}{\omega_r}\right)^2} \right| \tag{5}$$

where ω_h is the frequency of the lowest order harmonic current generated by the converter.

The relationship between I_{hs}/I_h and ω_h/ω_r is also plotted and given in Fig. 4. It would be considered appropriate that the frequency of the lowest order harmonic current ω_h is selected at least twice as high as the system resonant frequency ω_r, that is, $\omega_h > 2\,\omega_r$, at which I_{hs} is substantially attenuated as indicated in Fig. 4 (point *Q*). Therefore, the resonant frequency can be determined by

$$\omega_r < \frac{\omega_h}{2} \tag{6}$$

from which the value of the capacitor can be calculated by

$$C_s > \frac{4}{\omega_h^2 L_s}. \tag{7}$$

For the converter using switching pattern *A* with $L_s = 0.15$ pu and $\omega_h = 11$ pu, the value of the capacitor is $C_s > 0.22$ pu.

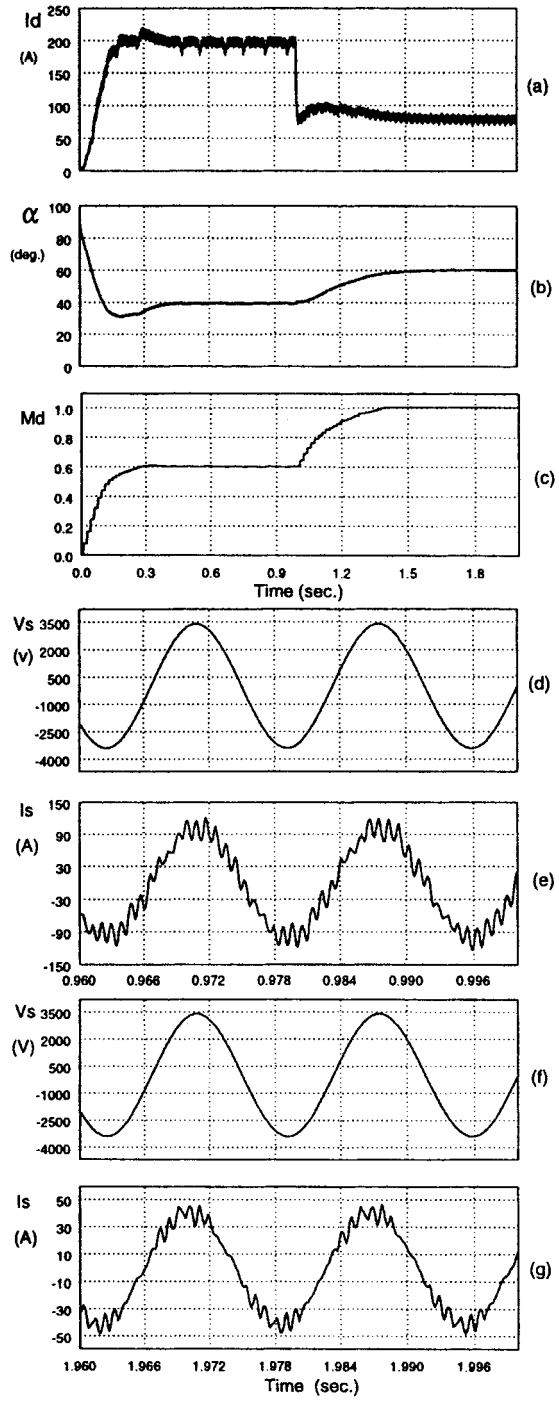

Fig. 6. Simulation results ($f_{sw} = 600$ Hz). At $t = 1.0$ s, $I_d = 1.0$ pu, $M_d = 0.6$, and $PF = 1.0$. At $t = 2.0$ s, $I_d = 0.4$ pu, $M_d = 1.0$, and $PF = 0.965$ (highest possible value).

IV. Proposed Power Factor Control Scheme

Based on the principle of maximum power factor control discussed in the previous sections, a novel power factor control scheme, shown in Fig. 5, is proposed. In a feedforward loop, the detected phase angle Φ between the source voltage V_s and current I_s is compared with the phase angle reference Φ^* which is usually set at zero degree, requesting unity power factor operation. The resultant error signal is used to control modulation index M_d. In the feedback loop, the dc current I_d is compared with the current reference I_d^*. The error signal is used to control delay angle α. It should be noted that the magnitude of dc current I_d is actually controlled by both feedforward and feedback loops.

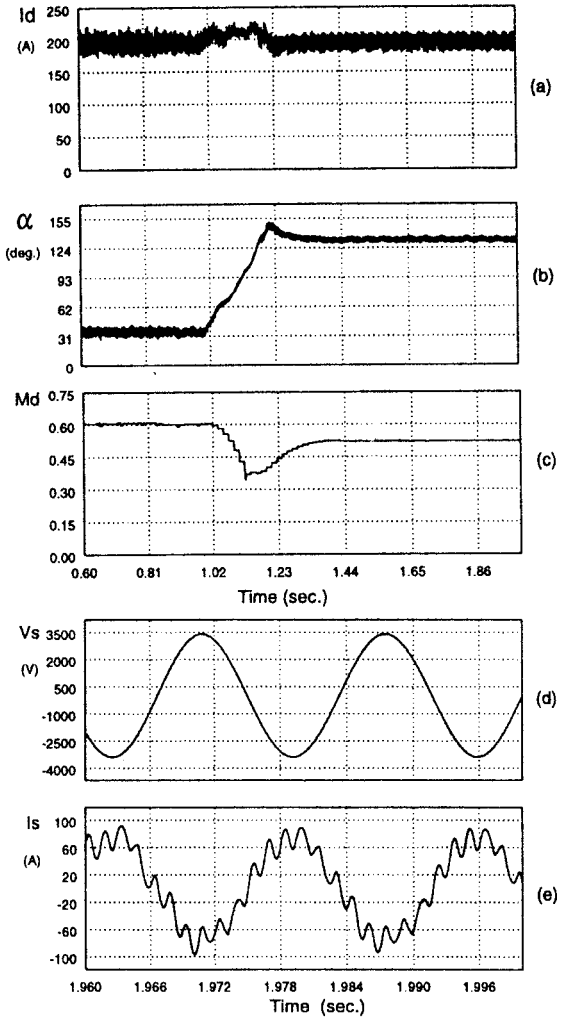

Fig. 7. Simulation of regenerating operation ($f_{sw} = 360$ Hz).

The proposed control scheme can guarantee the system input power factor is unity as long as the maximum value of M_d is not reached. Assuming that the source current I_s leads voltage V_s by an angle due to a change in load, an error signal $\Phi^* - \Phi$ will be generated. This error signal will result in a higher modulation index M_d, which, in turn, will increase the dc current I_d. The increase in I_d will cause the feedback loop to respond. The delay angle α will be spontaneously increased to keep I_d at a value set by the current reference I_d^*. The increase in α will reduce the phase angle ϕ between I_s and V_s. This process continues until the unity power factor is reached, at which I_s is in phase with V_s and the converter is running at a new operating point.

Under certain operating conditions (e.g., a light load), where unity power factor is not achievable, the source current I_s will

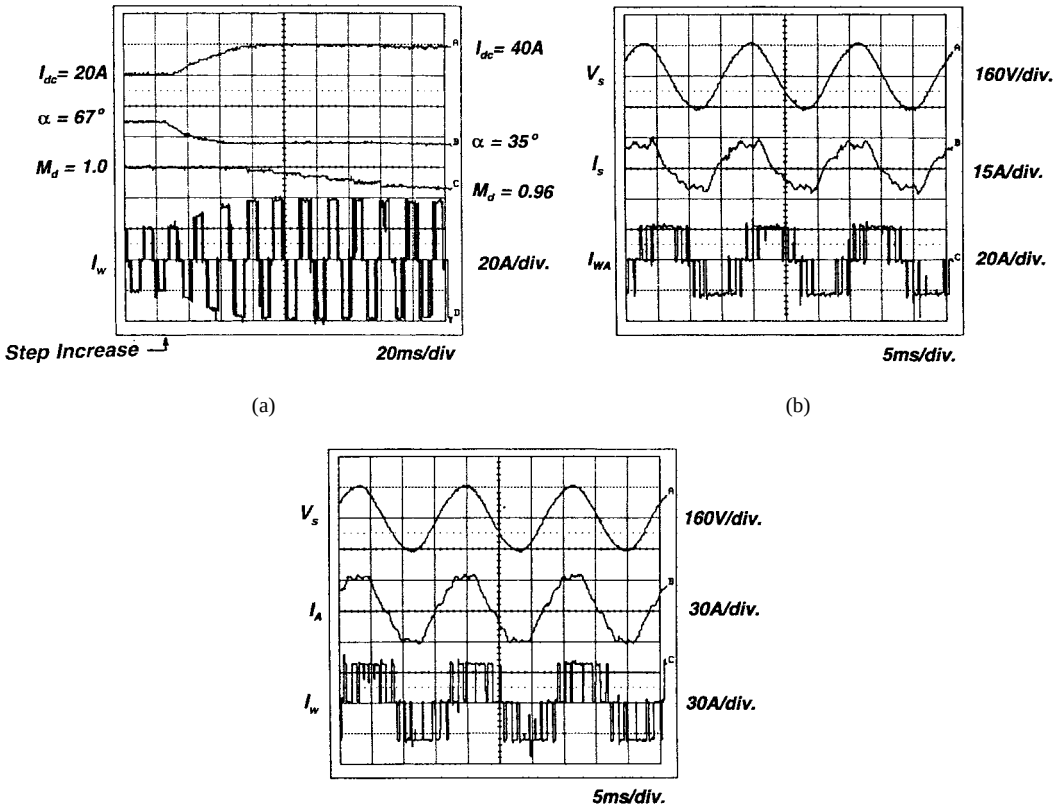

Fig. 8. Experimental results. (a) Waveforms with a step increase in reference current I_d^* at $t = 25$ ms. (b) $PF = 0.93$ with $I_d = 20$ A (before the step increase in I_d^*. (c) $PF = 1.0$ with $I_d = 40$ A (after the step increase in I_d^*.

lead voltage V_s by an angle Φ which cannot be reduced to zero. In this case, the output of the proportional integral (PI) regulator for M_d control will keep increasing, which, in turn, will keep the delay angle α increasing through the feedback loop in order to maintain a constant dc current set by I_d^*, until the PI regulator is saturated. At this point, M_d reaches its maximum value and the delay angle α also reaches a value that will produce the highest possible input power factor. Obviously, the transition between the unity and maximum power factor operations is smooth and automatic. No extra measures should be taken, which is one of the features of this scheme.

V. Simulation and Experimental Results

Fig. 6 shows a set of simulated transient and steady-state waveforms of the converter system under different operating conditions. The converter is rated at 4160 V, 60 Hz, and 1000 kVA with $L_s = 0.05$ and $C_s = 0.4$ per unit. The switching frequency of the converter is 600 Hz with 5th, 7th, 11th, and 13th harmonic elimination (switching pattern *B*). At $t = 1.0$ s, the converter reaches a steady-state operating point where $I_d = I_d^* = 1.0$, $V_d = 0.5$, and $R_L = 0.5$, all in per unit. As shown in Fig. 6(b) and (e), the input (displacement) power factor is unity with $M_d = 0.603$ and $\alpha = 39.6°$. At $t > 1.0$ s, the current reference I_d^* is reduced to 0.4 pu and, at the same time, the load resistance is increased to 1.25 pu to keep the dc voltage at 0.5 per unit. At $t = 2.0$ s, when the system reaches a new steady state, the modulation index M_d is saturated and the delay angle α is 60.27°, at which a maximum power factor is obtained. In this case, the phase angle Φ between V_s and I_s is 15.1°, as indicated in Fig. 6(f) and (g), and the power factor reaches a value of 0.965, which corresponds to point *P* in Fig. 3.

The proposed control scheme can also produce a unity power factor when the converter operates in a regeneration mode. The regeneration occurs when the dc voltage changes its polarity. For example, in an induction motor drive where the GTO converter is used as a front-end converter, the dc voltage will go negative when the energy generated by the motor or its mechanical load is fed back to the ac mains. Fig. 7 illustrates such a case. The parameters used in simulation remain the same as those used in Fig. 6, except switching pattern *A* is used with a switching frequency of 360 Hz. Accordingly, the line reactance is adjusted from 0.05 to 0.15 pu. At $t = 1.0$ s, the converter reaches a steady-state operating point where $I_d = I_d^* = 1.0$, $V_d = 0.5$, and $R_L = 0.5$, all in per unit. To simulate regenerating operation, the load voltage starts to decrease at $t = 1.0$ s and then reaches -0.8 pu at 1.2 s. When steady state is reached at 2.0 s, the modulation index is lower than its maximum value, indicating that the power factor remains unity, as shown in Fig. 7(d) and (e).

Experimental results obtained from a laboratory GTO current-source converter are shown Fig. 8. The converter is rated at 208 V, 10 kVA, and 60 Hz with $L_s = 0.1$ pu

and $C_s = 0.6$ pu. The load resistance $R_L = 4\ \Omega$ (0.64 pu). The switching frequency of the converter is 360 Hz with fifth and seventh harmonic elimination. The converter initially operates with a load current of 20 A (0.5 pu). Under this operating condition, the unity power factor cannot be achieved, since the lagging component of the converter input current $I_w\,(I_w = 0.5\ M_d)$ is not large enough to completely compensate the leading component generated by the capacitor ($I_c = 0.6$ pu). Mathematically, (1) does not have a solution, since the term of $\omega_s C_s V_s/(M_d I_d) = 0.6/0.5 = 1.2$. In this case, the PI controller for the M_d control is saturated, keeping M_d at its maximum value of 1.0. The delay angle α is automatically adjusted by its PI controller to 67°, at which the dc current is kept at a value set by the current reference I_d^*, [refer to Fig. 8(a), prior to a step increase in I_d^*, and Fig. 8(b)]. The (displacement) power factor is kept at a maximum achievable value of 21.6° ($PF = 0.93$), instead of 75° ($PF = 0.26$) produced by a scheme with M_d control alone.

The unity power factor can be achieved when the load current is increased. This can be done by increasing the reference current I_d^*. The corresponding experimental waveforms are also shown in Fig. 8, where the load current is increased to 40 A (1.0 pu) and M_d is decreased from its maximum value to 0.96 [Fig. 8(a)] and the input power factor reaches unity [Fig. 8(c)].

It should be pointed out that the term "power factor" used in this paper is, in fact, the displacement factor. Considering the fact that the converter input current I_w is close to sinusoidal due to the use of PWM techniques and the line capacitor, the distortion factor is negligible. Therefore, the differences among the power factor, displacement factor, and distortion factor are not distinguished in this paper.

VI. Conclusions

A novel power factor control scheme has been proposed for high-power GTO current-source converters. In this scheme, the converter input power factor is controlled by two PI regulators, one in a feedforward loop for modulation index control and the other in a feedback loop for delay angle control. The input power factor can be kept at unity or its highest possible value. Compared with other schemes proposed in the literature, this scheme does not require any system parameters. The power factor of the converter operated in a regenerating mode was investigated. The capacitor size and its effect are also discussed. Simulations on a 1-MVA converter and experimental results from a 10-kVA system are provided to verify the operating principle of the scheme. This scheme is particular suitable for high-power (500 kVA and up) converters where a large-size (0.2–0.6 pu) capacitor has to be used, which has an adverse effect on system input power factor.

Appendix
Per-Unit System

The per-unit system is usually based on converter ratings. As an example, the per-unit system and its associated base values used in the simulation of this paper are defined as follows:

converter ratings—4160 V/1000 kVA

$$
\begin{aligned}
V_{\text{base, L–L}} &= V_{\text{rated, L–L}} = 4.16 \text{ kV} \\
S_{\text{base}} &= S_{\text{rated}} = 1.0 \text{ MVA} \\
\omega_{\text{base}} &= \omega_{\text{rated}} = 3.77 \text{ rad/s} \\
Z_{\text{base}} &= \frac{V_{\text{base, L–L}}^2}{S_{\text{base}}} = \frac{4.16^2}{1.0} 17.3\ \Omega \\
C_{\text{base}} &= \frac{1}{(377 \times 17.3)} = 153.3\ \mu\text{F} \\
L_{\text{base}} &= \frac{17.3}{377} = 45.9 \text{ mH} \\
C_{\text{pu}} &= \frac{C}{C_{\text{base}}} \\
L_{\text{pu}} &= \frac{L}{L_{\text{base}}}.
\end{aligned}
$$

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Yuan Xiao, for a photograph and biography, see p. 884 of the July/August 1998 issue of this Transactions.

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