

Structure Generation and Design of Multiple Loop Feedback OTA-Grounded Capacitor Filters

Yichuang Sun, *Member, IEEE*, and J. Kel Fidler

Abstract—This paper addresses the structure generation, analysis and synthesis of multiple loop feedback OTA-C filters. A systematic approach is proposed for all-pole filters, and the generation and design of minimum component structures are extensively exemplified. Two general methods for transmission zero realization are also suggested and two architectures with simple design formulas are illustrated. Using the theory many new interesting configurations can be produced alongside some known structures. All the filter architectures contain only grounded capacitors and all internal nodes in canonical realizations have a grounded capacitor. A general method for sensitivity analysis of the structures is formulated. Numerical design examples and simulation results are also presented. The essence of the theory is the establishment of the relationship between the filter structure and the feedback matrix, which makes systematic structure generation and general design equation formulation possible.

Index Terms—Active filters, analog circuit design, analog signal processing, continuous-time filters, OTA-C filters.

I. INTRODUCTION

ACTIVE FILTER DESIGN has been thoroughly investigated for operational voltage amplifier based active- RC filters. Three well-known methods, that is, the cascade of biquadratic sections, simulation based on passive LC ladder prototypes, and the multiple loop feedback have been very well established [1]. However, it has been found that op amp based active- RC filters are not suitable for high frequency operation, fully integrated implementation, and electronic tuning, and frequently are based on complex structures.

Tremendous efforts have therefore been made over recent years to develop new alternative techniques in high frequency continuous-time filters. The OTA-C approach, in particular, uses the operational transconductance amplifier to displace the conventional operational voltage amplifier and associated resistors in active- RC filters and has achieved outstanding performance improvement in structural simplicity, electronic tunability, high frequency capability, and monolithic integrability. This technique has hence received most attention [2] and has become today the main approach for high-frequency full-integration filtering.

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Y. Sun is with the Department of Electrical and Electronic Engineering, University of Hertfordshire, Hatfield Herts AL 10 9AB, U.K.

J. K. Fidler is with the Department of Electronics, University of York, York YO1 5DD, U.K.

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At present the performance of low-order OTA-C filters has been proved and a body of literature has been published for the design of second-order OTA-C filters [3]–[8]. Research has turned to the realization of high-order specifications [8]–[21]. For high-order OTA-C filter synthesis, cascade design based on biquadratic sections has been most widely used. Research has been directed to simulation techniques [9]–[11] as well. Some researchers have also explored the feedback coupled-biquad method [12], [13], although this well-known filter design method has not received equal attention, compared with the other two. No matter what the approach, the filter structures almost always consist of integrators and amplifiers as the most basic building blocks, and have feedback loops in this basic level. A general approach may be therefore developed based on the multiple loop feedback structure constructed with integrators and amplifiers.

Practical considerations in high frequency OTA-C filter design may specify using grounded capacitors and reducing the number of components. The former is because the grounded capacitor can be implemented on a smaller area than the floating counterpart and it can absorb equivalent shunt capacitive parasitics. The latter is due to the fact that a large number of components may increase power consumption, chip areas, noise, and parasitic effects. Thus the design method and resulting filter structures should be based on grounded capacitors and canonical architectures, although noncanonical realizations may be required in some situations to achieve design flexibility or to satisfy some special specifications.

This paper will show how to generate, analyze and design multiple integrator loop feedback filter structures using OTA's and grounded capacitors for synthesis of both transmission poles and zeros. General theory with a systematic scheme for generating all-pole filter structures is established in Section II, with concentration on minimum component OTA-C realizations in Section III, where the exhaustive enumeration of canonical filter structures is investigated. Section IV introduces two general methods for generation of transmission zeros, together with illustrative examples. In Section V general sensitivity relations are established and Section IV presents some design and simulation examples. The paper concludes with a brief summary and some further comments.

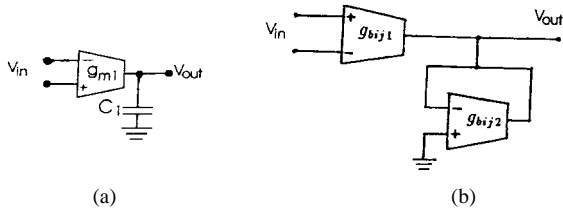


Fig. 1. OTA-C building blocks: integrator and amplifier.

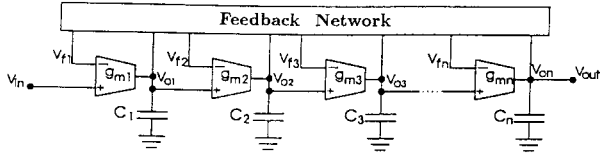


Fig. 2. Multiple loop feedback OTA-C filter model.

II. GENERAL THEORY OF MULTIPLE LOOP FEEDBACK OTA-C FILTERS

A. Multiple Loop Feedback OTA-C Filter Model

The basic building blocks in the construction of OTA-C filters are integrators and amplifiers as shown in Fig. 1(a) and (b), respectively. The voltage transfer functions $H(s) = V_{\text{out}}/V_{\text{in}}$ (V_{in} is the noninverting voltage minus the inverting voltage of the related OTA) of the integrator and amplifier are simply shown as $H(s) = 1/(sC_1/g_{m1})$ and $H(s) = g_{bi,j1}/g_{bi,j2}$, respectively.

The general multiple integrator loop feedback OTA-C model with all capacitors being grounded to be addressed in the paper is shown in Fig. 2. As depicted, this model is composed of a feedforward network consisting of n OTA-C integrators connected in cascade and a feedback network that may contain OTA voltage amplifiers and/or pure wire connections.

B. System Equations and Transfer Function

To generally analyze the model, the feedback network may be described as

$$V_{fi} = \sum_{j=i}^n f_{ij} V_{oj}, \quad i = 1, 2, \dots, n \quad (1)$$

where f_{ij} is the voltage feedback coefficient from the output of integrator j to the input of integrator i . The coefficient f_{ij} can have zero and nonzero values, depending on whether there is an open circuit or an amplifier (gain $g_{bi,j1}/g_{bi,j2}$) between the i th and j th integrators, respectively. The former means no feedback exists, while the latter suits any amount of feedback. In particular, for the direct feedback connection we may have the unity feedback $f_{ij} = 1$.

Equation (1) can also be written in the matrix form.

$$V_f = FV_o \quad (2)$$

where $V_o = [V_{o1} \ V_{o2} \ \dots \ V_{on}]^t$, the output voltage vector of integrators, $V_f = [V_{f1} \ V_{f2} \ \dots \ V_{fn}]^t$, the feedback voltage vector to the negative input terminals of integrators, and $F = [f_{ij}]_{n \times n}$, the feedback coefficient matrix. The superscript t stands for transpose.

The currents flowing into and out of the feedback network all are zero, since they are related to the input terminals of the OTA's in the feedforward circuit or in the feedback network, which are ideally infinite impedance. Noting this and denoting time constants $\tau_j = C_j/g_{mj}$, we can write the equations for the feedforward network by inspection

$$\begin{aligned} s\tau_1 V_{o1} &= V_{\text{in}} - V_{f1} \\ s\tau_{j+1} V_{oj+1} &= V_{oj} - V_{fj+1} \end{aligned} \quad (3)$$

where s is the complex frequency.

Equation (3) can also be condensed in a matrix form

$$V_o = M(s)^{-1}(IV_{\text{in}} - V_f) \quad (4)$$

where the superscript -1 represents the inversion operation and

$$M(s) = \begin{bmatrix} s\tau_1 & & & & \\ -1 & s\tau_2 & & & \\ & -1 & s\tau_3 & & \\ & & & \ddots & \\ & & & & -1 & s\tau_n \end{bmatrix} \quad (5)$$

$$I = [1 \ 0 \ \dots \ 0]^t. \quad (6)$$

Combining (2) and (4) we can obtain the equation for the whole system as

$$A(s)V_o = IV_{\text{in}} \quad (7)$$

where the system coefficient matrix

$$A(s) = M(s) + F. \quad (8)$$

Equation (7) establishes the relationship between the overall circuit input and the integrator outputs including the overall circuit output. Using this equation we can formulate the circuit transfer function. Solving (7) yields

$$\begin{aligned} \frac{V_o}{V_{\text{in}}} &= A(s)^{-1}I \\ &= \frac{1}{|A(s)|} \begin{bmatrix} A_{11}(s) \\ A_{12}(s) \\ \vdots \\ A_{1n}(s) \end{bmatrix} \end{aligned} \quad (9)$$

where $|A(s)|$ and $A_{ij}(s)$ represent the determinant and cofactors of $A(s)$, respectively.

Since the overall circuit output $V_{\text{out}} = V_{on}$, from (9) it can be readily identified that the system transfer function is given by $H(s) = V_{\text{out}}/V_{\text{in}} = A_{1n}(s)/|A(s)|$. Noting the structural feature of $M(s)$ and that F is an upper triangular matrix, using (8) we can demonstrate that $A_{1n}(s) = 1$. Thus the transfer function $H(s)$ can be simplified as

$$H(s) = \frac{1}{|A(s)|} \quad (10)$$

C. Feedback Coefficient Matrix and Systematic Generation of Filter Structures

The feedback matrix F is defined by (2) and has the property that

$$f_{ij} \begin{cases} \neq 0 & \text{if there is feedback between } V_{fi} \text{ and } V_{oj}, \\ = 0 & \text{otherwise} \end{cases}$$

As can be seen from (2), if all the elements in a row of F , say row i , are zero, the corresponding feedback voltage V_{fi} will be zero and so is the converse. $V_{fi} = 0$ means that the inverting terminal of the OTA in the i th integrator is grounded.

Note that F is an upper triangular matrix; for all nonzero elements f_{ij} there are $i \leq j$. If we further suppose that no inverting integrator terminals are grounded, the feedback matrix will also have the property that each row has one and only one nonzero element, which implies that f_{nn} is always nonzero. The nonzero feedback coefficient can be realized using an OTA voltage amplifier and the unity feedback coefficient can also be achieved using pure wire connection, as an alternative to using a unity gain amplifier.

In the following by the canonical or minimum component realization we mean that for realizing the unity DC gain n th-order all-pole low-pass filter, only n OTA's and n capacitors (i.e., n integrators) are required [14], [15]. For the general model in Fig. 2 the canonical realization is clearly equivalent to no components existing in the feedback network. Alternatively we can say that for canonical architectures, the feedback matrix $F = [f_{ij}]_{n \times n}$ defined by (2) obviously has only zero and unit elements, since feedback can only be achieved by direct connection.

It is apparent that there is an one-to-one correspondence between the feedback matrix F and the circuit configuration and different F will give rise to different circuit structures. To show this we consider the situation that feedback is realized only by direct connection and none of the OTA inverting terminals in the integrators are grounded. According to the features of the general F discussed above, the feedback matrix F now becomes an upper triangular (0, 1) matrix and has one and only one unit element in each row, leading to $f_{nn} = 1$. Therefore for the n th-order model there are $n!$ combinations of unit element positions in the matrix. Note that the unit element $f_{ij} = 1$ in each combination is realized by a direct connection between the negative input terminal of integrator i and the output of integrator j . Thus we have $n!$ different combinations of feedback connections, i.e., $n!$ different filter structures.

It is of particular interest that this also suggests a method for generating all possible filter architectures that are canonical and without grounded integrator inverting terminals. That is, for any given order n , we first find all $n!$ combinations of unit element positions in F . Direct connections are then made corresponding to all unit feedback coefficients in each combination; this is repeated for all $n!$ different combinations. This method is extensively studied and exemplified in Section III.

D. Filter Synthesis Procedure Based on Coefficient Matching

From (5) and (8) we can see that the determinant $|A(s)|$ may normally be an n th-order polynomial of s . The trans-

fer function in (10) may therefore have the all-pole filter characteristic.

The general form of all-pole low-pass transfer functions can be expressed as

$$H_d(s) = \frac{A_0}{B_n s^n + B_{n-1} s^{n-1} + \dots + B_1 s + 1}. \quad (11)$$

To synthesize this desired function $H_d(s)$ we may follow the generic procedure shown below.

Based on (10), by expansion of $|A(s)|$ we attain the circuit transfer function

$$H(s) = \frac{g_0(\tau_h, f_{ij})}{g_n(\tau_h, f_{ij})s^n + g_{n-1}(\tau_h, f_{ij})s^{n-1} + \dots + g_1(\tau_h, f_{ij})s + 1}. \quad (12)$$

Comparing (11) and (12), to achieve the desired characteristic the following set of coefficient matching equations must be satisfied:

$$\begin{aligned} g_n(\tau_h, f_{ij}) &= B_n \\ g_{n-1}(\tau_h, f_{ij}) &= B_{n-1}, \dots \\ g_1(\tau_h, f_{ij}) &= B_1 \\ g_0(\tau_h, f_{ij}) &= A_0. \end{aligned} \quad (13)$$

Solving (13) we obtain τ_h and f_{ij} . To finish the design we compute the values of each C and g from τ_j and f_{ij} .

The efficient expansion of $|A(s)|$ to reach the polynomial form in s of (12) is the first step in the design. Some symbolic analysis techniques may be required generally to deal with $|A(s)|$ to get coefficient matching equations. However, the issue may be quite easily handled for low-order and some general high-order filters as will be shown in the next section.

The coefficient match equations are usually nonlinear. Note that to produce the item s^k , there is at least one group of k integrators making a multiplicative contribution to the corresponding coefficient. Hence $g_k(\tau_h, f_{ij})$ will contain at least one term of multiplication of k integration constants τ_h . In most cases a nonlinear equation solver may be invoked to solve the derived parameter value determination equations. In Section III we will show that the design equations of many structures can also be easily solved explicitly.

To further determine each g and C there exist n degrees of freedom in the canonical realization and more than n degrees in the noncanonical. Thus the transconductances or the capacitances can be arbitrarily assigned to be identical. Taking the canonical realization as an example we may set $g_{m1} = g_{m2} = \dots = g_{mn} = g_m$ and then calculate $C_j = g_m \tau_j$, for any j or let $C_1 = C_2 = \dots = C_n = C$ and then compute $g_{mj} = C/\tau_j$.

As can be seen from (8) the network performance is a function of F . Different F will lead to different transfer characteristics in (10). F is also linked with filter structures and different F will correspond to different architectures. Thus the relationship between the performance and the structure is established through the feedback matrix. The significance is even more in that the generality and systematicity of the design method is obtained due to the introduction of F .

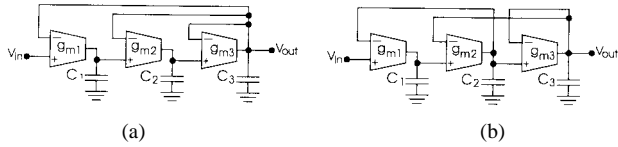


Fig. 3. Third-order canonical OTA-C filters.

III. STRUCTURE AND DESIGN OF ALL-POLE OTA-C FILTERS

In this section, we exemplify the application of the general method proposed in Section II. For simplicity and clarity, we concentrate on exhaustive search of all possible canonical filter configurations with no feedback voltages being grounded for a given order n using the method given in Section II-C. Some component value determination formulas are also presented.

A. Third-Order OTA-C Filters

For the third-order model that is a derivative version of Fig. 2 corresponding to $n = 3$, with general F and using (10) we formulate the general transfer function as

$$H(s) = 1 / \{ \tau_1 \tau_2 \tau_3 s^3 + (\tau_1 \tau_2 f_{33} + \tau_1 \tau_3 f_{22} + \tau_2 \tau_3 f_{11}) s^2 + [\tau_1 (f_{22} f_{33} + f_{23}) + \tau_2 f_{11} f_{33} + \tau_3 (f_{11} f_{22} + f_{12})] s + (f_{11} f_{22} f_{33} + f_{11} f_{23} + f_{12} f_{33} + f_{13}) \}. \quad (14)$$

As proved in Section II-C, there are altogether six possible configurations. It can be verified that the last item in the denominator of (14) is equal to 1 for all the structures, and so $A_0 = 1$ in (11).

When $f_{13} = f_{23} = f_{33} = 1$ and the other elements are zero, we have the structure in Fig. 3(a) and the circuit transfer function in (14) becomes

$$H(s) = \frac{1}{\tau_1 \tau_2 \tau_3 s^3 + \tau_1 \tau_2 s^2 + \tau_1 s + 1}. \quad (15)$$

The parameter value equations are demonstrated as

$$\begin{aligned} \tau_1 &= B_1 \\ \tau_2 &= \frac{B_2}{B_1} \\ \tau_3 &= \frac{B_3}{B_2}. \end{aligned} \quad (16)$$

If we select $f_{12} = f_{23} = f_{33} = 1$ and the other $f_{ij} = 0$, the filter architecture in Fig. 3(b) results. The corresponding transfer function and the parameter value determination formulas are derived as

$$H(s) = \frac{1}{\tau_1 \tau_2 \tau_3 s^3 + \tau_1 \tau_2 s^2 + (\tau_1 + \tau_3) s + 1} \quad (17)$$

$$\begin{aligned} \tau_3 &= \frac{B_3}{B_2} \\ \tau_2 &= \frac{B_2}{B_1 - \frac{B_3}{B_2}} \\ \tau_1 &= B_1 - \frac{B_3}{B_2}. \end{aligned} \quad (18)$$

For F with $f_{11} = f_{23} = f_{33} = 1$ and the other $f_{ij} = 0$, or $f_{12} = f_{22} = f_{33} = 1$ and the other $f_{ij} = 0$, the circuits

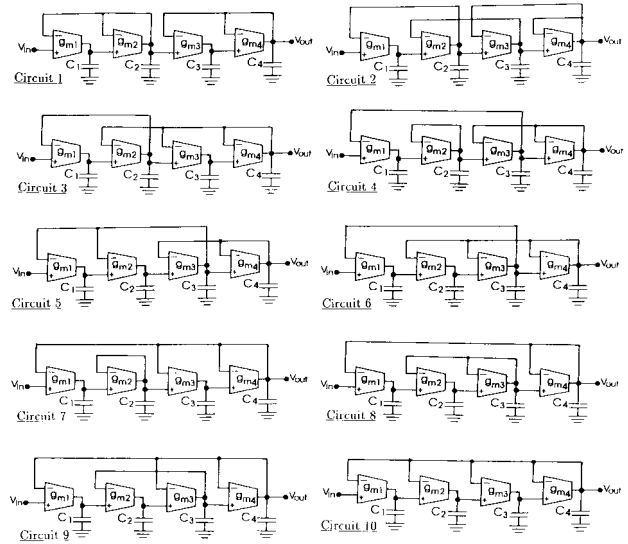


Fig. 4. Fourth-order all-pole canonical OTA-C filter structures.

become cascaded by a first-order and a second-order canonical sections.

The other two combinations do not seem practical. When F is a unity matrix, the structure becomes a cascade of three first-order canonical sections, which can only realize some real poles. The structure corresponding to $f_{13} = f_{22} = f_{33} = 1$ and the other $f_{ij} = 0$ has no solutions for the Butterworth and Chebyshev approximations, which has been numerically verified, and therefore is also rejected.

B. Fourth-Order OTA-C Filters

For the fourth-order general model of Fig. 2, again from (8) and (10) the general transfer function can be written with some tedious manipulation as

$$H(s) = 1 / \{ (\tau_1 \tau_2 \tau_3 \tau_4) s^4 + (\tau_1 \tau_2 \tau_3 f_{44} + \tau_1 \tau_2 \tau_4 f_{33} + \tau_1 \tau_3 \tau_4 f_{22} + \tau_2 \tau_3 \tau_4 f_{11}) s^3 + [\tau_1 \tau_2 (f_{33} f_{44} + f_{34}) + \tau_1 \tau_3 f_{22} f_{44} + \tau_1 \tau_4 (f_{22} f_{33} + f_{23}) + \tau_2 \tau_3 f_{11} f_{44} + \tau_2 \tau_4 f_{11} f_{33} + \tau_3 \tau_4 (f_{11} f_{22} + f_{12})] s^2 + [\tau_1 (f_{22} f_{33} f_{44} + f_{22} f_{34} + f_{23} f_{44} + f_{24}) + \tau_2 (f_{11} f_{33} f_{44} + f_{11} f_{34}) + \tau_3 (f_{11} f_{22} f_{44} + f_{12} f_{44}) + \tau_4 (f_{11} f_{22} f_{33} + f_{11} f_{23} + f_{12} f_{33} + f_{13})] s + (f_{11} f_{22} f_{33} f_{44} + f_{11} f_{22} f_{34} + f_{11} f_{44} f_{23} + f_{12} f_{33} f_{44} + f_{11} f_{24} + f_{13} f_{44} + f_{12} f_{34} + f_{14}) \}. \quad (19)$$

For any particular F we can easily draw the associated structure, obtain the corresponding transfer function, and calculate the component values. There are altogether 24 combinations of possible filter configurations according to the discussion in Section II-C. Ten practical structures are shown in Fig. 4 and the corresponding F 's, transfer functions, and some design formulas are presented below. Note that in each case the f_{ij} 's that are not written out are treated as zero and the realization of the unity dc gain all-pole characteristic in (11) with $A_0 = 1$ is dealt with.

Circuit 1: $f_{12} = f_{22} = f_{34} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + (\tau_1 \tau_2 \tau_3 + \tau_1 \tau_3 \tau_4) s^3 + (\tau_1 \tau_2 + \tau_1 \tau_3 + \tau_3 \tau_4) s^2 + (\tau_1 + \tau_3) s + 1].$$

Circuit 2: $f_{12} = f_{23} = f_{34} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + \tau_1 \tau_2 \tau_3 s^3 + (\tau_1 \tau_2 + \tau_1 \tau_4 + \tau_3 \tau_4) s^2 + (\tau_1 + \tau_3) s + 1]$$

$$\begin{aligned} \tau_4 &= \frac{B_4}{B_3} \\ \tau_3 &= \frac{B_3}{B} \\ \tau_2 &= \frac{B}{B_1 - \frac{B_3}{B}} \\ \tau_1 &= B_1 - \frac{B_3}{B} \\ B &= B_2 - \frac{B_1 B_4}{B_3}. \end{aligned} \quad (20)$$

Circuit 3: $f_{12} = f_{24} = f_{34} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + \tau_1 \tau_2 \tau_3 s^3 + (\tau_1 \tau_2 + \tau_3 \tau_4) s^2 + (\tau_1 + \tau_3) s + 1]$$

$$\begin{aligned} \tau_4 &= \frac{B_4}{B_3} \\ \frac{B_4}{B_3} \tau_3^2 - B_2 \tau_3 + B_3 &= 0 \\ \tau_2 &= \frac{B_2 - \frac{B_4}{B_3} \tau_3}{B_1 - \tau_3} \\ \tau_1 &= B_1 - \tau_3. \end{aligned}$$

Circuit 4: $f_{13} = f_{22} = f_{34} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + (\tau_1 \tau_2 \tau_3 + \tau_1 \tau_3 \tau_4) s^3 + (\tau_1 \tau_2 + \tau_1 \tau_3) s^2 + (\tau_1 + \tau_4) s + 1].$$

Circuit 5: $f_{13} = f_{23} = f_{34} = f_{44} = 1$

$$H(s) = \frac{1}{\tau_1 \tau_2 \tau_3 \tau_4 s^4 + \tau_1 \tau_2 \tau_3 s^3 + (\tau_1 \tau_2 + \tau_1 \tau_4) s^2 + (\tau_1 + \tau_4) s + 1}$$

$$\begin{aligned} \tau_4 &= \frac{B_4}{B_3} \\ \tau_3 &= \frac{B_3}{B_2 - \frac{(B_1 - \frac{B_4}{B_3}) B_4}{B_3}} \\ \tau_2 &= \frac{B_2}{B_1 - \frac{B_4}{B_3}} - \frac{B_4}{B_3} \\ \tau_1 &= B_1 - \frac{B_4}{B_3} \end{aligned}$$

Circuit 6: $f_{13} = f_{24} = f_{34} = f_{44} = 1$

$$H(s) = \frac{1}{\tau_1 \tau_2 \tau_3 \tau_4 s^4 + \tau_1 \tau_2 \tau_3 s^3 + \tau_1 \tau_2 s^2 + (\tau_1 + \tau_4) s + 1}$$

$$\begin{aligned} \tau_4 &= \frac{B_4}{B_3} \\ \tau_3 &= \frac{B_3}{B_2} \\ \tau_2 &= \frac{B_2}{B_1 - \frac{B_4}{B_3}} \\ \tau_1 &= B_1 - \frac{B_4}{B_3}. \end{aligned}$$

Circuit 7: $f_{14} = f_{22} = f_{34} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + (\tau_1 \tau_2 \tau_3 + \tau_1 \tau_3 \tau_4) s^3 + (\tau_1 \tau_2 + \tau_1 \tau_3) s^2 + \tau_1 s + 1]$$

$$\begin{aligned} \tau_1 &= B_1 \\ B_1 \tau_2^3 - B_2 \tau_2^2 + B_3 \tau_2 - B_4 &= 0 \\ \tau_3 &= \frac{B_2}{B_1} - \tau_2 \\ \tau_4 &= \frac{\frac{B_4}{B_1}}{\tau_2 \left(\frac{B_2}{B_1} - \tau_2 \right)}. \end{aligned}$$

Circuit 8: $f_{14} = f_{23} = f_{33} = f_{44} = 1$

$$H(s) = 1 / [\tau_1 \tau_2 \tau_3 \tau_4 s^4 + (\tau_1 \tau_2 \tau_3 + \tau_1 \tau_2 \tau_4) s^3 + (\tau_1 \tau_2 + \tau_1 \tau_4) s^2 + \tau_1 s + 1]$$

$$\begin{aligned} \tau_1 &= B_1 \\ B_1 \tau_4^3 - B_2 \tau_4^2 + B_3 \tau_4 - B_4 &= 0 \\ \tau_2 &= \frac{B_2}{B_1} - \tau_4 \\ \tau_3 &= \frac{\frac{B_4}{B_1}}{\tau_4 \left(\frac{B_2}{B_1} - \tau_4 \right)}. \end{aligned}$$

Circuit 9: $f_{14} = f_{23} = f_{34} = f_{44} = 1$

$$H(s) = \frac{1}{\tau_1 \tau_2 \tau_3 \tau_4 s^4 + \tau_1 \tau_2 \tau_3 s^3 + (\tau_1 \tau_2 + \tau_1 \tau_4) s^2 + \tau_1 s + 1}$$

$$\begin{aligned} \tau_4 &= \frac{B_4}{B_3} \\ \tau_3 &= \frac{B_3}{B_2 - \frac{B_1 B_4}{B_3}} \\ \tau_2 &= \frac{B_2}{B_1} - \frac{B_4}{B_3} \\ \tau_1 &= B_1. \end{aligned}$$

Circuit 10: $f_{14} = f_{24} = f_{34} = f_{44} = 1$

$$H(s) = \frac{1}{\tau_1\tau_2\tau_3\tau_4s^4 + \tau_1\tau_2\tau_3s^3 + \tau_1\tau_2s^2 + \tau_1s + 1}$$

$$\begin{aligned}\tau_1 &= B_1 \\ \tau_2 &= \frac{B_2}{B_1} \\ \tau_3 &= \frac{B_3}{B_2} \\ \tau_4 &= \frac{B_4}{B_3}.\end{aligned}$$

It is observed that Circuits 2, 3, 5, 6, 9, and 10 can be easily designed using the attached formulas. Circuits 7 and 8 need the solution of a cubic equation. Circuit 1 can be solved either by the factorization method or a nonlinear equation solver. The nonlinear equation algorithm is also needed in the design of Circuit 4.

In addition to the ten configurations presented above there are another 14 possible structures. These 14 configurations, however, have been found not suitable for realizing the Butterworth and Chebyshev approximations; 10 of them are a cascade of canonical sections of either four first-orders, or two first-orders and one second-order, or one first-order and one third-order, which cannot realize two pairs of complex poles, while the other 4 (corresponding to $f_{12} = f_{24} = f_{33} = f_{44} = 1$, $f_{13} = f_{24} = f_{33} = f_{44} = 1$, $f_{14} = f_{22} = f_{33} = f_{44} = 1$, and $f_{14} = f_{24} = f_{33} = f_{44} = 1$, respectively) have no practical solutions of the associated design equations.

C. General n th-Order Architectures

General n th-order architectures can also be derived in a similar way. Rather than trying to exhaustively enumerate all $n!$ possible general structures due to the complexity of the problem, we present some typical ones for the illustrative purpose.

If F is chosen so that the elements in the last column all are unity and the other elements of the matrix are zero, then the circuit has the inverse follow-the-leader-feedback (IFLF) structure [15], whose third-order version has also been given in Fig. 3(a) and fourth-order counterpart is Circuit 10 in Fig. 4. The general design formulas can be explicitly obtained for this n th-order IFLF circuit [15], [17], as will also be given in Section IV.

If the choice is made of $f_{i(i+1)} = 1$, $i = 1, 2, \dots, n-1$, $f_{nn} = 1$, and all the other f_{ij} 's are zero, then the leapfrog (LF) configuration results [15]. The derivative third- and fourth-order counterparts have been exhibited in Fig. 3(b) and in Circuit 2 of Fig. 4, respectively. (We may note that the third-order low-pass OTA-C filter in [18] and the ladder simulation filter in [9] also belong to the LF structure category.)

Finally when n is even and

$$F = \text{diag} \left\{ \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \right\}$$

the circuit becomes cascaded biquadratic sections, with the i th section being the canonical structure. The fourth-order case has been shown in Fig. 4, that is, Circuit 1.

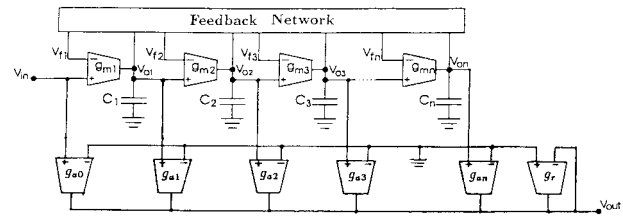


Fig. 5. OTA-C filter model with output summation OTA network.

Although only canonical structures with integrator inverting input terminals being ungrounded are illustrated, it should be noted that the explicit expressions of transfer function of the third- and fourth-order models given in (14) and (19) are general; they are actually suitable for any realizations of feedback coefficients. If some or all feedback coefficients are realized with OTA voltage amplifiers or grounded integrator inverting terminals are allowed, more structure varieties can of course be obtained. For example, if we select $f_{1j} \neq 0$, $j = 1, 2, \dots, n$ and the other $f_{ij} = 0$, with f_{1j} being realized by OTA voltage amplifiers, then the general FLF structure can be obtained.

IV. GENERATION AND SYNTHESIS OF TRANSMISSION ZEROS

In this section we address the issue of implementing the transmission zeros, that is, the synthesis of the general transfer function:

$$H(s) = \frac{A_n s^n + A_{n-1} s^{n-1} + \dots + A_1 s + A_0}{B_n s^n + B_{n-1} s^{n-1} + \dots + B_1 s + 1}. \quad (21)$$

For a given input to some node, different nodes may support different types of output characteristic, while for a fixed output node the output function may vary as the input node changes. Therefore by altering the input and output nodes we may realize some transmission zeros.

More generally, for a given input we may combine the different node outputs with a summation OTA network to give the overall circuit output, or for a fixed output distribute the overall input onto different circuit nodes using an OTA distribution network. A general transfer function can thus be obtained. Then by properly selecting the summation or distribution weights for respective cases one may attain any filter characteristics. In the following we will formulate only design equations of the two methods. Detailed particulars concerning the realization of various numerator characteristics using different architectures will not be given, because of the length of the paper.

A. Output Summation of OTA Network

Here we connect a summation OTA network to the circuit in Fig. 2, as shown in Fig. 5. Denoting $H_j(s) = V_{o,j}/V_{in}$ and $k_j = g_{a,j}/g_r$ we derive

$$\begin{aligned}H(s) &= \frac{V_{out}}{V_{in}} \\ &= k_0 + \sum_{j=1}^n k_j H_j(s).\end{aligned} \quad (22)$$

Using the results given in Section II-B (9) we know that

$$H_j(s) = \frac{A_{1j}(s)}{|A(s)|}. \quad (23)$$

Substituting (23) into (22) we have the circuit transfer function

$$H(s) = k_0 + \frac{1}{|A(s)|} \sum_{j=1}^n k_j A_{1j}(s). \quad (24)$$

The overall transfer function in (24) may have the general form of (21) with reference to matrix $A(s)$ in (8) and the transmission zeros may be controlled arbitrarily by transconductances g_{aj} through weights k_j .

As an illustration, for the canonical IFLF structure ($f_{jn} = 1$, $j = 1, 2, \dots, n$ and the other $f_{ij} = 0$) with the output summation OTA network [20], using (8) we can demonstrate

$$|A(s)| = \tau_1 \tau_2 \cdots \tau_n s^n + \tau_1 \tau_2 \cdots \tau_{n-1} s^{n-1} + \cdots + \tau_1 \tau_2 s^2 + \tau_1 s + 1 \quad (25)$$

$$A_{1j}(s) = \tau_{j+1} \tau_{j+2} \cdots \tau_n s^{n-j} + \tau_{j+1} \tau_{j+2} \cdots \tau_{n-1} s^{n-j-1} + \cdots + \tau_{j+1} \tau_{j+2} s^2 + \tau_{j+1} s + 1 \quad (26)$$

where $j = 1, 2, 3, \dots, n-1$.

Substitution of relations (25) and (26) into (24) yields the general circuit transfer function and comparing this function with that in (21) we have the design equations:

$$B_j = \prod_{i=1}^j \tau_i, \quad (j = 1, 2, \dots, n) \quad (27)$$

$$A_{n-j} = \sum_{i=0}^j \left(k_i \prod_{h=i+1}^{n-j+i} \tau_h \right), \quad (j = 0, 1, 2, \dots, n-1)$$

$$A_0 = \sum_{i=0}^n k_i. \quad (28)$$

From the design viewpoint if the transfer characteristic of (21) is desired the circuit parameters must then be determined in terms of coefficients A_j and B_j from (27) and (28). With $B_0 = 1$ it is easy to demonstrate that

$$\tau_j = \frac{B_j}{B_{j-1}}, \quad (j = 1, 2, 3, \dots, n) \quad (29)$$

$$A_{n-j} = \sum_{i=0}^j \left(\frac{B_{n-j+i}}{B_i} \right) k_i, \quad (j = 0, 1, 2, \dots, n). \quad (30)$$

Equation (29) can be directly used for calculation of integration constants τ_j . From (30) the iterative computation formulas of summation weights k_j can also be obtained, given by

$$k_0 = \frac{A_n}{B_n}$$

$$k_j = \frac{B_j}{B_n} \left[A_{n-j} - \sum_{i=0}^{j-1} \left(\frac{B_{n-j+i}}{B_i} \right) k_i \right] \quad (j = 1, 2, 3, \dots, n). \quad (31)$$

The parameter value determination formulas in (29) and (31) apply to any order realizations, including the second-order [5].

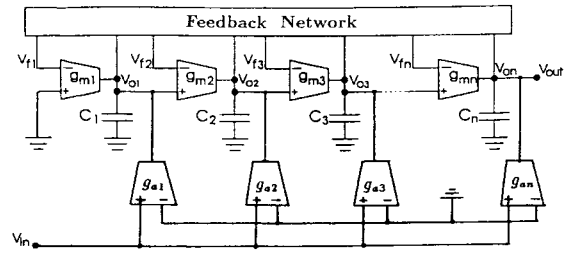


Fig. 6. OTA-C filter model with input distribution OTA network.

It can be observed from numerator coefficient expressions (28) or (30) that the circuit may realize any special transfer functions, since we can enable any coefficient A_i of the numerator to be any value including zero by properly choosing the values and signs of g_{aj} , $j \leq n-i$. On the other hand, for any required zeros, that is, any values of A_i we can easily compute the associated parameters k_j by means of (31). If the calculated k_j is negative, we can simply interchange the two input terminals of the related OTA with g_{aj} . If the computed value of k_j is zero, then the g_{aj} OTA should be removed. Similarly we may also realize any special biquadratic filters by appropriately selecting g_{aj} , $j = 0, 1, 2$ [5].

B. Input Distribution of OTA Network

In this approach, the voltage signal is applied to circuit nodes by an input OTA network as shown in Fig. 6. The exactly same formulation process as that in Section II-B can be followed to derive the design equations for this case. All the relations in (1), (2), (4), (5), (7), and (8) apply here, with only one exception that instead of $I = [1 \ 0 \ \cdots \ 0]^t$ of (6) in Section II-B, now

$$I = [\beta_1 \ \beta_2 \ \cdots \ \beta_n]^t \quad (32)$$

where $\beta_j = g_{aj}/g_{mj}$, since (3) in Section II-B becomes for the present case

$$s\tau_1 V_{o1} = \beta_1 V_{in} - V_{f1}$$

$$s\tau_{j+1} V_{oj+1} = \beta_{j+1} V_{in} + (V_{oj} - V_{fj+1}). \quad (33)$$

This exception is clearly due to the change of input form; in Fig. 2 the input voltage is applied onto only the first integrator output node and this is realized directly through the OTA in the integrator, while in the present case the input voltage is distributed onto all the integrator output nodes and this is accomplished by extra OTA's.

First solving (7) for V_o , then substituting (32) and finally observing $V_{out} = V_{on}$ we can formulate that

$$H(s) = \frac{V_{out}}{V_{in}}$$

$$= \frac{1}{|A(s)|} \sum_{j=1}^n \beta_j A_{jn}(s). \quad (34)$$

Note that $A_{ij}(s)$ is at least one order less in s than $|A(s)|$. The expression in (34) offers transfer functions of less than n th order numerators. Now we consider the canonical IFLF

B. Sensitivities of Third- and Fourth-Order Filters

The general τ_j sensitivity functions of the third-order structure are derived using (41).

$$\begin{aligned} S_{\tau_1}^H(s) &= -H(s)[\tau_1\tau_2\tau_3s^3 + (\tau_1\tau_2f_{33} + \tau_1\tau_3f_{22})s^2 \\ &\quad + \tau_1(f_{22}f_{33} + f_{23})s] \\ S_{\tau_2}^H(s) &= -H(s)[\tau_1\tau_2\tau_3s^3 + (\tau_1\tau_2f_{33} + \tau_2\tau_3f_{11})s^2 \\ &\quad + \tau_2f_{11}f_{33}s] \\ S_{\tau_3}^H(s) &= -H(s)[\tau_1\tau_2\tau_3s^3 + (\tau_1\tau_3f_{22} + \tau_2\tau_3f_{11})s^2 \\ &\quad + \tau_3(f_{11}f_{22} + f_{12})s] \end{aligned}$$

where $H(s)$ has been given in (14) in Section III-A.

When realizing the unity dc gain characteristic ($A_0 = 1$) in (11), the sensitivities for $f_{13} = f_{23} = f_{33} = 1$ and the other $f_{ij} = 0$ in F , i.e., the configuration in Fig. 3(a), are calculated with substitution of (16), given by

$$S_{\tau_h}^H(s) = -\frac{\sum_{j=h}^3 B_j s^j}{\sum_{j=1}^3 B_j s^j + 1}, \quad h = 1, 2, 3.$$

For F with $f_{12} = f_{23} = f_{33} = 1$ and the other $f_{ij} = 0$, i.e., the structure in Fig. 3(b), with incorporation of (18) the sensitivities can also be readily derived [14].

Now consider the fourth-order canonical LF structure, Circuit 2 in Fig. 4. Again, based on the general relation in (41) and when the filter realizes the unity dc gain all-pole characteristic in (11), the sensitivity functions to τ_j are demonstrated, with (20) being incorporated, as

$$\begin{aligned} S_{\tau_1}^H(s) &= -\frac{B_4s^4 + B_3s^3 + \left(B_2 - \frac{B_4}{B}\right)s^2 + \left(B_1 - \frac{B_3}{B}\right)s}{D_d(s)} \\ S_{\tau_2}^H(s) &= -\frac{B_4s^4 + B_3s^3 + Bs^2}{D_d(s)} \\ S_{\tau_3}^H(s) &= -\frac{B_4s^4 + B_3s^3 + \frac{B_4}{B}s^2 + \frac{B_3}{B}s}{D_d(s)} \\ S_{\tau_4}^H(s) &= -\frac{B_4s^4 + \frac{B_1B_4}{B_3}s^2}{D_d(s)} \\ D_d(s) &= B_4s^4 + B_3s^3 + B_2s^2 + B_1s + 1 \\ B &= B_2 - \frac{B_1B_4}{B_3}. \end{aligned}$$

From the sensitivity functions developed above, we may easily obtain the magnitude and the phase sensitivities of $H(j\omega)$, since they are the real and imaginary parts of $S_x^H(j\omega)$ (x is τ_i or f_{ij}), respectively. The Schoeffler's measure [1] can also be readily calculated by

$$S = \sum_{i=1}^n |S_{\tau_i}^H(j\omega)|^2 + \sum_{i=1}^n \sum_{h=1, h \geq i}^n |S_{f_{ih}}^H(j\omega)|^2. \quad (45)$$

TABLE I
PARAMETER VALUES FOR NORMALIZED FOURTH-ORDER BUTTERWORTH FILTER

Circuit	τ_1	τ_2	τ_3	τ_4
1	0.765 367	1.306 56	1.847 76	0.541 196
2	1.847 76	0.541 196	0.765 367	1.306 56
3	1.530 73	1.577 16	1.082 39	0.382 683
4	1.767 63	1.748 47	0.845 492	0.382 683
5	1.945 3	0.896 275	0.858 833	0.667 826
6	2.230 44	1.148 05	1.020 49	0.382 683
7	2.230 44	1.530 73	0.765 367	0.382 683
8	2.613 13	0.667 368	0.639 195	0.8971
9	2.613 13	0.639 195	0.8971	0.667 368
10	2.613 13	0.923 88	1.082 39	0.382 683
11	2.613 13	1.306 56	0.765 367	0.382 683

VI. DESIGN AND SIMULATION EXAMPLES

All the examples in Sections III–V for all-pole filters, finite transmission zero filters, and sensitivity calculation, respectively have been confirmed by direct routine circuit analysis. This straightforward confirmation also intuitively verifies the correctness of the general relations established in Sections II–V. In this section we further give some numerical and simulation results.

A. Numerical Design Examples

For the fourth-order Butterworth low-pass filter the normalized transfer function is

$$H_d(s) = \frac{1}{s^4 + 2.61313s^3 + 3.41421s^2 + 2.61313s + 1}.$$

We use the ten canonical structures given in Fig. 4 in Section III-B to realize this characteristic. Identifying that $B_4 = 1$, $B_3 = B_1 = 2.61313$, and $B_2 = 3.41421$, the parameter values of the structures are calculated by using the formulated explicit solutions or the nonlinear equation solving approach, which are given in Table I.

In Table I we list two sets of solutions for Circuit 1 in Fig. 4. This is because the two biquadratic sections in the circuit are interchangeable in cascade order. We have also realized the Chebyshev filters using the structures in Fig. 4 [15].

B. Sensitivity Analysis Results

For the fourth-order LF canonical Butterworth filter, substituting $B_4 = 1$, $B_3 = B_1 = 2.61313$, $B_2 = 3.41421$ into the expressions in Section V-B and utilizing (45) (where the second part is now zero) the Schoeffler's multiparameter sensitivity is computed as shown in Fig. 7.

C. Frequency Performance Simulation

The realization of the fourth-order 455 kHz unity gain Butterworth filter using the LF structure (Circuit 2) in Fig. 4 is simulated. The equal transconductance design is adopted with the transconductance value being $g_m = 30.14 \mu\text{S}$. The normalized capacitances are calculated as $C_1 = 46.136$, $C_2 = 47.536$, $C_3 = 32.623$, and $C_4 = 11.534 \mu\text{F}$ from the corresponding data in Table I. For the cut-off frequency 455 kHz, frequency denormalization leads to the nominal circuit capacitances $C_1 = 16.138$, $C_2 = 16.628$, $C_3 = 11.411$,

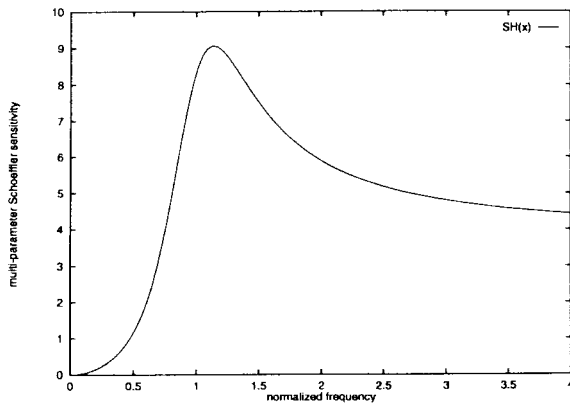


Fig. 7. Schoeffler's multiparameter sensitivity of fourth-order canonical LF structure.

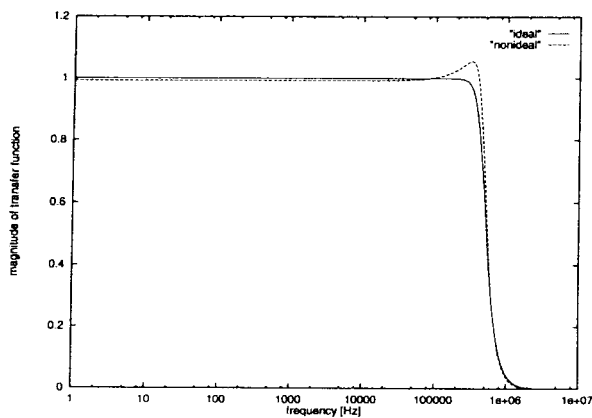


Fig. 8. Simulated frequency response of fourth-order Butterworth LF filter.

and $C_4 = 4.035$ pF. The simulated magnitude frequency response is shown in Fig. 8, which is the same as the expected characteristic.

The nonideal performance is also simulated. The macro-model of the CMOS OTA [18] with the differential-mode input capacitance $C_{id} = 0.0385$ pF, the common-mode input capacitance $C_{ic} = 0.0502$ pF, the output conductance $G_o = 113$ nS, the output capacitance $C_o = 0.52$ pF and the transconductance frequency dependence $G_m(s) = g_m(1 - sT_p)$ with $T_p = 21.2$ ns is utilized, which corresponds to the nominal transconductance value $30.14 \mu\text{S}$ [4]. The nonideal magnitude frequency response is also shown in Fig. 8, which shows that the simulated result agrees with the expected specification with slight deviation.

For the transmission zero realization, for example, using the input distribution method in Section IV, the reader may refer to [21], where a very detailed study of a third-order elliptic filter has been presented.

VII. CONCLUSIONS

A general multiple loop feedback approach for the realization of OTA-C filters has been proposed. The systematic generation, analysis and design of different filter configurations have been addressed. The method has the following advantages: a) it is systematic and general due to the introduction of the feedback matrix F and the relationship between F

and the feedback connection; b) a variety of new structures with different performances are generated, with both canonical and noncanonical realizations being available; c) all capacitors are grounded and canonical realization can guarantee that all internal nodes have a grounded capacitor; and d) it is also flexible in assigning element values and in various cases simple explicit design formulas are applicable.

We have formulated general relations for all-pole and finite transmission zero realizations. We have also demonstrated the general expressions for sensitivity computation. Using the one-to-one correspondence between the feedback connection matrix and the circuit configuration one can deal with any particular applications based on these general equations. For example, if the circuit topology is known, we may write the feedback matrix F and analyze the filtering characteristic and sensitivity performance. For the desired transfer function, on the other hand, an F , that is, a circuit structure, may be defined to realize the transfer function. In the paper extensive examples have been given. Although we have concentrated on the demonstration of the powerfulness of the proposed approach in generating high-order OTA-C filter structures, it is very obvious that some first- and second-order filters [3] can also be derived from the general model in Fig. 2.

The performance of multiple loop feedback OTA-C filters taking OTA nonidealities into account should be evaluated. OTA nonidealities may embrace finite input and output impedances, frequency dependence of transconductance, noise and nonlinearity of transconductance characteristic. They not only influence the frequency responses and pose stability problems, but also limit the filter dynamic range, as have been discussed in [21].

Noncanonical realization with OTA amplifiers realizing general feedback coefficients can provide some design flexibility and results in more useful architectures. However, the noncanonical synthesis produces some nonintegrating nodes (for example, if f_{ij} is realized with an OTA voltage amplifier, there will be a resistive node, which is the inverting input terminal of the i th integrator). The parasitic capacitances associated with the node may thus influence the high frequency performance, producing an unwanted pole. More OTA's also cause other problems as well; the total impact of OTA excess phases will dramatically increase, further degrading the high frequency performance, and larger chip areas and power consumption will also result. Since in the noncanonical realization some circuit node may connect more OTA's, the equivalent node conductance will be enhanced, which may severely deteriorate the low-frequency performance. In both canonical and noncanonical realizations the input capacitance of the integrator OTA will contribute to feedthrough effects (causing unwanted zeros). But in the canonical case it does not cause parasitic poles, since the OTA input capacitance is in a loop containing two circuit capacitances and the number of independent capacitances therefore remains the same.

There exists equivalent transformation of the structures with differential input OTA's and those with single input OTA's. Ideally a differential input OTA can be equivalent to two single input OTA's with the same transconductance value but opposite polarity. As discussed in [21], tradeoffs

between the feedthrough effects (parasitic zeros) caused by some differential input application and the large number of OTA's due to the single input application must be considered when deciding whether to exploit the differential or single input OTA's.

Balanced structures using differential input and differential output OTA's are popular in integrated implementation, which can achieve very high common-mode rejection ratio (CMRR) and reduce both the even-order harmonic distortion components and the effects of the power supply noise. The general unbalanced model in Fig. 2 can be converted into the balanced equivalent by using differential four input and two output OTA's in integrators and mirroring the feedback network in the upper part to the lower part. All the unbalanced configurations given in the paper can be thus converted into the corresponding balanced counterparts.

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Yichuang Sun (M'90) was born in Dalian, China, in 1960. He received the B.S. degree in radio communications and the M.S. degree in radio navigation from Dalian Maritime University, China, and the Ph.D. degree in electronic engineering from the University of York, U.K., in 1982, 1985, and 1996, respectively.

In 1985, he joined Dalian Maritime University, where since 1990, he has been an Associate Professor. He has held a research post at the University of York during the 1995–1996 academic year. He is currently on the staff of the University of Hertfordshire, U.K. His teaching and research interests include analog filter design, analog fault diagnosis, current-mode circuits, analog circuits and signal processing, RF circuits, circuit theory, computer-aided circuit design, and telecommunications and design. He has published more than 70 papers and received a number of awards and honors. His name has been included in three international Who's Who books.



J. Kel Fidler graduated from King's College, Durham University, and also the University of Newcastle.

He is Professor of electronics and Pro-Vice-Chancellor at the University of York, U.K., and has held posts at the University of Essex and the Open University. He has more than 30 years of research experience in the area of circuit theory, active and passive filter design, and computer-aided circuit design.

Professor Fidler was a past Chair of the IEE Professional Group E10 (Circuit Theory and Design), and was Chair of the ECCTD'88 Conference in Brighton, England. He is a Fellow of the Institute of Electrical Engineers, U.K.