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A New Technique for the Design of Multi-phase Voltage Controlled Oscillators

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In this work, a novel circuit structure for second-harmonic multi-phase voltage controlled oscillator (MVCO) is presented. The proposed MVCO is composed of N (N being an integer number and N≥ 2) identical inductor-capacitor (LC) tank VCOs. In theory, this MVCO can provide 2N different phase sinusoidal signals. A six-phase VCO based on the proposed structure is designed in a TSMC 0.18um CMOS process. Simulation results show that at the supply voltage of 0.8V, the total power consumption of the six-phase VCO circuit is about 1mW, the oscillation frequency is tunable from 2.3GHz to 2.5GHz when the control voltage varies from 0V to 0.8V, and the phase noise is lower than -128dBc/Hz at 1MHz offset frequency. The proposed MVCO has lower phase noise, lower power consumption and more outputs than other related works in the literature.

Keywords: Bulk-coupling; second-harmonic; low phase noise; low power consumption; Multi-phase Voltage Controlled Oscillator (MVCO).

1. Introduction

Radio Frequency (RF) voltage controlled oscillators (VCO) play a fundamental role in modern communications, signal processing, measurement systems and other applications. There are two popular types of RF VCO: ring oscillators [1-3] and negative resistance oscillators with inductor-capacitor (LC) tank [4-6]. Since the inductor of LC tank occupies large area, the ring oscillators have the advantage of smaller chip size [7]. However, owing to the high quality of the LC tank, LC oscillators are superior to ring oscillators in terms of phase noise and frequency performance, especially at high oscillation frequency. Thus, LC oscillators are widely used for high standard communications.

A multi-phase voltage controlled oscillator (MVCO) generally consists of several identical VCOs, being coupled through various ways. First, transistors [8] are often employed to produce multi-phase outputs, but this approach has the disadvantage of poor

phase accuracy. Second, transformers [9] are usually used for coupling for the advantage of wide tuning range and high swing amplitude, but this approach will degrade the phase noise performance of the circuit. The third approach is using capacitors for coupling [10]. This technique has the phase noise performance better than the transformer method, but it suffers from the disadvantage of lower tuning range. In this work, substrate [11] has been used for coupling. The substrate method can achieve low phase noise and low power consumption, thus a good candidate for high standard applications.

A LC-MVCO comprises several LC-VCOs connected in series from one oscillator to another. According to the operation mechanism, MVCOs can be classified into two categories: one category couples VCOs by injecting the fundamental frequency or first-harmonic signals from one LC tank to another [12], and the other category injects the second harmonic signals instead of the fundamental signals from the common node of each core oscillator to that of another. Compared with the first-harmonic approach, the second-harmonic MVCO has the advantage of better phase noise performance.

In this paper, a novel low phase noise second-harmonic multi-phase VCO is presented. Applying the proposed technique to couple three core VCOs, a six-phase VCO is obtained and designed. Simulations results are presented as well as comparison with the published works to verify the correctness and benefits of the proposed MVCO topology and design.

2. Circuit design and analysis

The schematic of the first-harmonic six-phase VCO (FSVCO) is shown in Fig.1, which consists of three identical LC-VCOs. Each VCO is composed of a cross-coupled pair of NMOS switching transistors (M_1-M_6) to provide negative impedance, an LC tank and the parallel connected NMOS transistors (M_7-M_{12}) for coupling. According to the simulation results which will be given later, 60^0 phase difference is achieved between the adjacent cells in steady state.

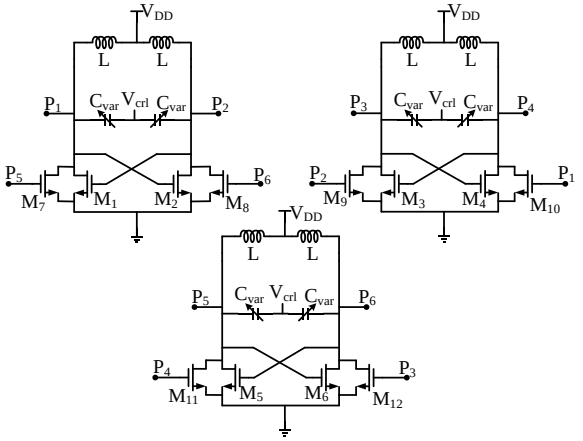

Fig.1. First-harmonic six-phase VCO.

In Fig.2, an improved multi-phase VCO structure with several modifications has been proposed to achieve better performance, which include: (1) super-harmonic technique is adopted for coupling, (2) all-PMOS structure and bulk-coupling technique are used for

better phase noise performance, and (3) tail resistor is utilized to achieve optimized swing amplitude [13]. The proposed MVCO is composed of N (N is an integer) core oscillators in a loop and 2N output signals with 2π/N phase shift (n = 0, 1, 2 … 2N-1) can be generated.

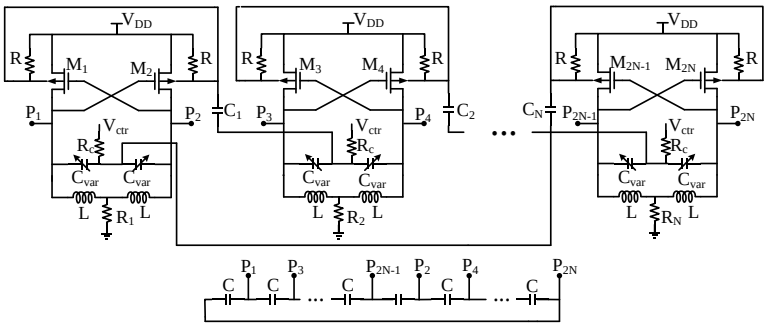

Fig.2. The schematic of the proposed MVCO.

For simplicity, applying the proposed technique to couple three LC-VCOs, a novel six-phase VCO is obtained as shown Fig.3. The proposed six-phase VCO is capable of generating six-phase sinusoidal outputs. The detailed design and analysis of the proposed six-phase VCO are given in the following.

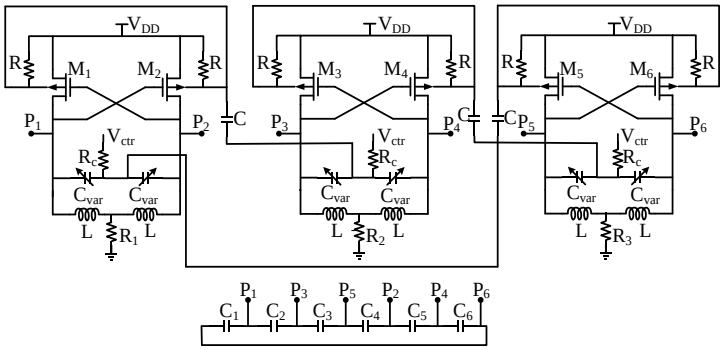

Fig.3. The schematic circuit of the proposed six phase VCO.

As deduced from [14], assume f_0 is the fundamental frequency of output voltages, then the dominant frequency at common source node under steady state is $2f_0$, which is called as second harmonic. Fig.4 shows the circuit of a LC-VCO, where the substrate node of the cross-coupled transistors act as the common source node. In this structure, the common source node is used for coupling. As shown in Fig.3, six-phase outputs are achieved by injecting the second-harmonic from one oscillator to the next, and the last oscillator injects the second-harmonic to the first oscillator.

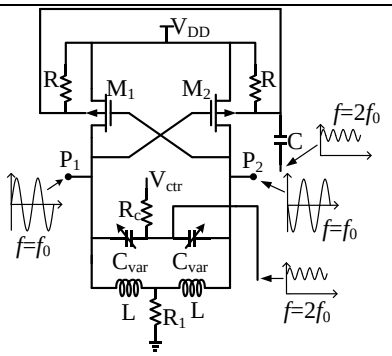

Fig.4. The circuit of a LC-VCO.

The phase variation through the loop is illustrated in Fig.5. Each LC-VCO has been modeled as a black box with two terminals oscillating at frequency $2f_0$. The three cores are placed in a loop and hence, based on the Barkhausen phase criterion, 360^0 phase deviation will exist around the loop. Thus:

$$\Delta\theta_1 + \Delta\theta_2 + \Delta\theta_3 + \Delta\theta_4 + \Delta\theta_5 + \Delta\theta_6 = 360^0 \tag{1}$$

The three LC-VCOs are assumed to be identical and thus the phase shifts caused by LC-tank are the same, that is:

$$\Delta\theta_1 = \Delta\theta_2 = \Delta\theta_3 \tag{2}$$

Owing to the symmetry of the circuit, the phase variations introduced by the coupling capacitors are also the same, hence:

$$\Delta\theta_4 = \Delta\theta_5 = \Delta\theta_6 \tag{3}$$

From (1)-(3), it is clear that:

$$\Delta\theta_1 + \Delta\theta_4 = \Delta\theta_2 + \Delta\theta_5 = \Delta\theta_3 + \Delta\theta_6$$
$$= (\Delta\theta_1 + \Delta\theta_2 + \Delta\theta_3 + \Delta\theta_4 + \Delta\theta_5 + \Delta\theta_6)/3 = 120^0 \tag{4}$$

From (4) we can conclude that 120^0 phase difference is obtained between the second harmonics, and therefore there is 60^0 phase shift between the first harmonics, which means a T/6 time shift between the waveforms at the adjacent output nodes.

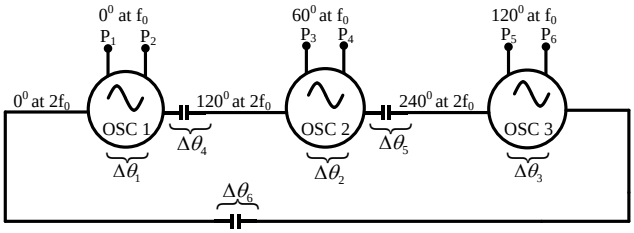

Fig.5. Six-phase LC VCO of three stages ring architecture.

There are several reasons for the superiority of the all-PMOS structure over the all-NMOS structure. Firstly, PMOS transistors exhibit better *1/f* noise than NMOS transistors; simulation results show that PMOS transistors exhibit about 10-dB less *1/f* noise compared

with NMOS transistors. Secondly, PMOS transistors also feature lower hot-carrier-induced white noise than NMOS transistors. Thirdly, the rise time and the fall time of PMOS transistors are more symmetrical to each other, which results in a smaller $1/f^3$ noise corner. As a result, all-PMOS-based VCOs can achieve better phase noise performance than all-NMOS structure, and therefore, in this paper, a new VCO core has been designed using a full PMOS transistor architecture.

The substrates of the MOS transistors are generally connected to their drain and source nodes or to V_{DD} (highest potential) for PMOS and GND (lowest potential) for NMOS. However, in the proposed MVCO, the substrate of the PMOS is used for coupling via a capacitor. In this structure, the coupling strength α can be optimized by choosing the values of resistor R and capacitor C. The resistors R are used for DC biasing of substrate terminals and the capacitors C are added for AC coupling. The phase accuracy that defines the availability of the phase difference from 60^0 between adjacent outputs is closely related to coupling strength factor α. Fig. 6(a) shows the proposed back-gate coupling VCO topology. Fig. 6(b) shows the equivalent small signal model for the circled part of the second-harmonic VCO in Fig. 6(a). From Fig. 6(b), the coupling strength α can be calculated by

$$\alpha = \frac{g_{mb1}}{g_{m1}} = \frac{\gamma_0}{2\sqrt{2\varphi_f - V_{BS}}} \tag{5}$$

where V_{BS} is the back-gate-to-source voltage, φ_f is a physical parameter, and γ_0 is a parameter determined by process. From (5), it is obvious that we can adjust α by changing V_{BS} in order to get optimized phase accuracy.

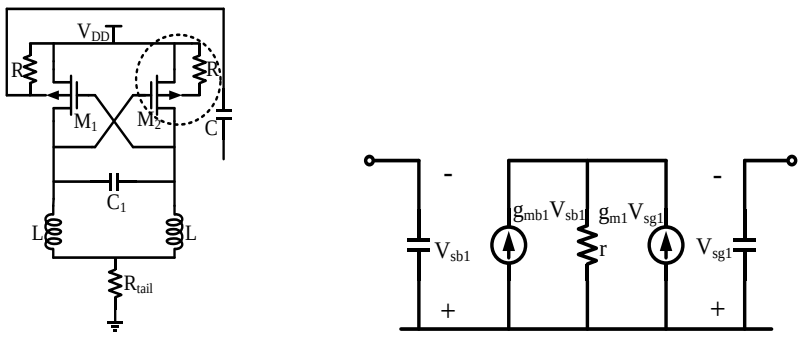

Fig.6. (a) The proposed back-gate coupling topology. (b) Small-signal equivalent circuit of the circled part in (a).

The advantage of using substrate for coupling is that it removes the additional transistors. In Fig.1, the noise produced by coupling transistors (M_7-M_{12}) may lead to phase jitter, subsequently resulting in the degradation in phase noise performance. In addition, the coupling transistors will consume some additional power and the feature size of the coupling transistors should be several times larger than the switching transistors to improve phase accuracy, but consequently, this causes an increase in parasitic capacitances which reduces the tuning range. In Fig.3, the coupling transistors are removed and the substrate of the PMOS is used as coupling components, so the coupling components are free of *1/f* noise. What's more, the usage of bulk coupling technique eliminates additional DC current path which is required for coupling, to reduce power consumption. So the proposed MVCO

can achieve lower power consumption and wider tuning range without sacrificing the phase noise performance compared with the transistor-based structure.

The capacitor coupling approach has a defect of no directivity preference to the multi-phases owing to unipolar capacitors. Capacitors C_1-C_6 are minimum size devices that are added to give proper directivity to the multi-phases. Without them, the oscillator would have no distinct preference for oscillation at either $+60^0$ or -60^0 phase difference. The current flowing through C_1-C_6 are negligible because the values of them are far lower than C.

Fig.7 shows the input resistance of a cross-coupled transconductor (devices M_1 and M_2) and its equivalent circuit.

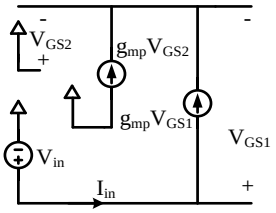

Fig.7. Equivalent circuit of the cross coupled transconductor.

In this work, the sizes of PMOS transistors are identical. Thus, the transconductances of M_1 and M_2 are the same as:

$$g_{mp1} = g_{mp2} = g_{mp} \tag{6}$$

According to the Kirchhoff 's law, we can get the following equations which are based on Fig.7:

$$I_{in} = g_{mp}V_{GS1} = -g_{mp}V_{GS2} \tag{7}$$

$$V_{in} = V_{GS1} - V_{GS2} \tag{8}$$

From (6), (7) and (8), the equivalent resistance produced by the cross-coupled PMOS pair can be derived as

$$R_{in} = V_{in}/I_{in} = -2/g_{mp} \tag{9}$$

From the analysis above, it is concluded that the equivalent impedance produced by the cross-coupled PMOS pair is a negative impedance. When increasing the dropout at M_1 and M_2, the output current is obtained to compensate for the loss of LC tank.

From Fig.3, we can see that the cross-coupled PMOS pair is in parallel with the LC tank. If $R_p \geq -2/g_{mp}$, the negative resistance can continuously afford energy to sustain oscillation.

In the range of state-of-the-art nanometer channel length, the threshold voltage V_{th} of MOSFET is not constant due to the short-channel and narrow-channel effects. It can be adjusted by changing circuit parameters such as channel width, gate length and drain-to-source voltage, which is given by (10) [15]

$$V_t = V_{t0} + \gamma[(|2\Phi_F + V_{SB}|)^{0.5} - (|2\Phi_F|)^{0.5}] \tag{10}$$

where:

V_{SB} = the electric potential difference between source and substrate;
V_{t0} = the threshold voltage when V_{SB} = 0 V;
γ = the bulk effect coefficient, with a typical value in the range of 0.3 ~ $0.4V^{0.5}$; and
Φ_F = a physical parameter with typical value of 0.3 V.

From (10), it is obvious that increasing the voltage at substrate terminal results in decrease in V_{BS}, leading to lower threshold voltage (V_{th}). In this work, the substrate of PMOS transistors is tied to V_{DD} via a resistor, resulting in lower threshold voltage than regular switching transistors. Therefore, lower power consumption can be achieved by adopting forward bias technique (shown in Fig.8). Furthermore, a resistor R serves as a part of a highpass filter (HPF) coupling network with the value of 10kΩ for the purpose of preventing signal leakage.

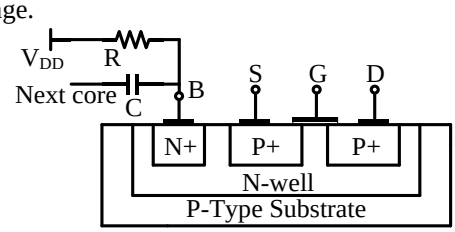

Fig.8. The representation of the forward body bias technique.

3. Simulation results

The proposed low power low phase noise six-phase VCO is designed and simulated using TSMC 0.18μm RF CMOS process. Thanks to the forward body bias technique used, the supply voltage can reduce to 0.8V. The power consumption of the proposed MVCO is about $1mW$. The transistors sizes are $(W/L = 10\mu m/0.18\mu m)$. The load resistor (R_1, R_2, R_3) is about 50Ω, which can ensure the optimum swing amplitude. The values of the other components are L=2.5nH, R=10kΩ, C=1pF.

Fig.9-14 are the post-layout simulation results of the six-phase VCO. Fig.9 shows the transient waveform of $P_{1\text{-}6}$ during their initial time. It can be observed that the starting time to oscillate is about 7us. Fig.10 shows the multi-phase outputs at their steady state. As can be seen from Fig.10, the oscillation frequency is about 2.4GHz.

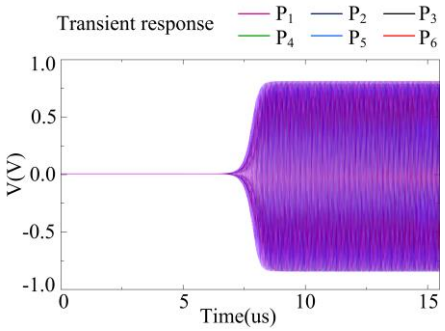

Fig.9. The waveform of $P_{1\text{-}6}$ during initial time.

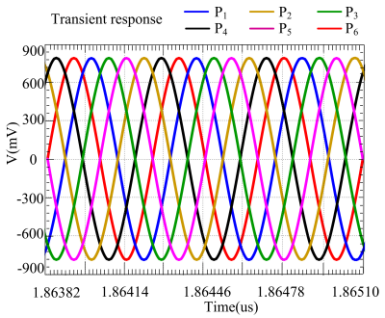

Fig.10. The waveform of $P_{1\text{-}6}$ during steady state.

Fig.11 shows the output frequency versus the control voltage when the supply voltage is 0.8V. It is observed that when changing the control voltage from 0V to 0.8V, the output frequency varies from 2.32GHz to 2.45GHz.

Fig.12 shows phase noise performance of the proposed six-phase oscillator. As can be seen from marker M_0, the phase noise of the proposed MVCO at 1MHz offset is -128dBc/Hz when oscillating at 2.4GHz.

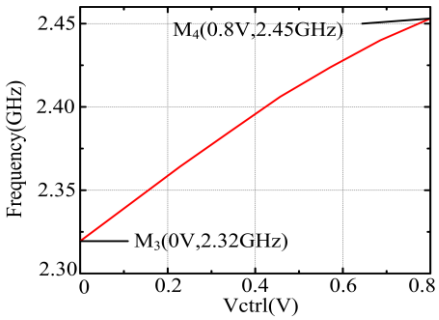

Fig.11. The output frequency versus control voltage.

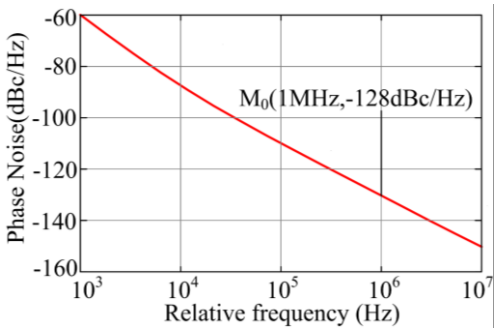

Fig.12. The phase noise of the proposed MVCO.

Fig.13 shows Monte Carlo simulations to measure phase mismatch errors due to 3% device mismatches in inductors, transistors and capacitors and 0.5% width mismatch in varactors in the six-phase VCO outputs for 200 samples. The simulated 3σ phase errors are 0.51° at 0.8V supply.

Fig.14 shows the output frequency variations of the six-phase VCO when temperature varies from -20℃ to 80℃ (step size=10℃) for three process corners: FF, TT, SS (only PMOS-FETs are included in this circuit). From Fig.14, it is obvious that the maximum frequency deviation is about 65MHz or within 2.7% of the nominal value (2.4GHz). Therefore, it is a reliable signal generator.

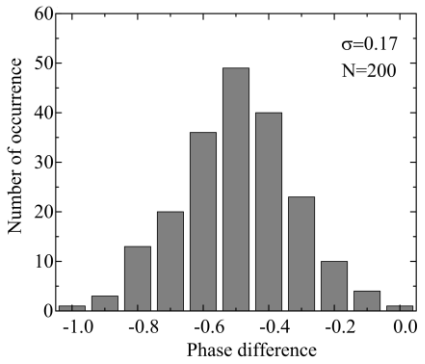

Fig.13. Monte Carlo simulation on phase difference for 200 samples.

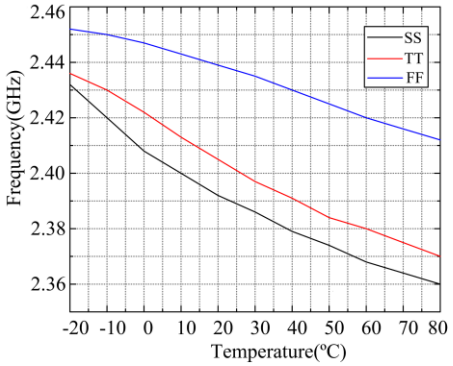

Fig.14. Output frequency dependent on process and temperature.

Here, a commonly used figure of merit (*FOM*) which takes oscillation frequency, power consumption and phase noise into account has been adopted to compare the proposed work with other reported and related works.

$$FOM = \mathrm{L}(\Delta\omega) + 20\log\left(\frac{\Delta\omega}{\omega}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (11)$$

where $\Delta\omega$ stands for the offset angular frequency, ω is the angular oscillation frequency, P_{DC} is the DC power consumption measured in milliwatts. $L(\Delta\omega)$ is the phase noise measured at offset frequency $\Delta\omega$ from the carrier frequency. The lower value of *FOM* means the better performance.

Table 1 summarizes the performances of the proposed MVCO compared with other published works. The results show that the proposed MVCO has a good overall performance in terms of supply voltage, power consumption, phase noise, and the number of multi-phase output.

Table. 1. Performance comparison with related published works.

Reference	Technology (nm)	V_{DD} (V)	Tuning range(GHz)	Power (mW)	Number of output	Phase noise(dBc/Hz at 1MHz offset)	Figure of merit
[16]	650	0.6	2.75-6.25	5.8	4	-123.7	-185
[17]	650	1.2	48.8-62.3	15.6	4	-96	-179
[18]	130	1.8	5.05-5.84	11.25	4	-116.4	-181
[19]	180	1.2	2.5-2.97	3.6	4	-126.8	-189
[20]	130	1	4.4-5.4	4.2	4	-121	-189
[21]	180	1.05	5.8-6.44	2.0	4	-117.7	-190
[22]	180	1.6	9.4-10.1	2.88	4	-106.9	-182
FSVCO	180	1.2	2.1-2.65	1.8	6	-118	-183
This work	180	0.8	2.32-2.45	1	6	-128	-194

4. Conclusion

In this paper we have proposed a novel general MVCO structure. The proposed MVCO is able to produce multi-phase signals. Several techniques have been introduced to improve the overall performance to meet the requirements of high standard applications. A six-phase VCO has been designed and simulated at 2.4GHz oscillation frequency and 0.8V supply voltage. The results indicate low phase noise and low power consumption. A detailed comparison with the published works has also been given

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