Design of a Fourth-Order Continuous-Time Filter for UWB Receivers

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***Abstract*– The design and implementation of a CMOS current-mode fourth-order Butterworth continuous-time leap-frog (LF) multiple loop feedback (MLF) lowpass filter is described. The filter is implemented using a fully-differential linear, low voltage and low power operational transconductance amplifier (OTA). PSpice simulations using a standard TSMC 0.18μm CMOS process with 1.5V power supply have shown that the cut-off frequency of the filter ranges from 240MHz to 300MHz and dynamic range is about 58dB at 240MHz of cut-off frequency. The power consumption of the filter is only from 22.3 to 55mW. The total output noise density is about 390nA/√Hz.**

I. INTRODUCTION

Ultra wideband (UWB) is an upcoming standard for short-range, high data rate communications link. Recently, UWB technologies have attracted considerable attention [1]. In order to achieve the highest integration for UWB receivers, the direct down-conversion architecture is used. As can be seen from the Figure 1, the analogue baseband block of the receiver is composed of variable gain amplifiers (VGA) and lowpass filters. The VGAs increase the signal amplitude, while the lowpass filter reduces the amount of the out-of-band signal in order to increase the dynamic range available for the useful signal. The VGA design has been well studied in the literature [2, 3]. For UWB analogue front-end, the variable gain range does not need to be very large; thus the implementation of VGA is not critical. Therefore, the lowpass filter design becomes the most critical in the analogue baseband. The Gm-C based lowpass filter is the only option as the cut-off frequency of filter access to a few hundred megahertz. Although there are a few high performances Gm-C filter can be also found in the literature [4-10], they all suffer from the relatively high power consumptions. In order to minimize the power consumption, both operational transconductance amplifiers (OTAs) and filters need to be designed carefully. At the OTA design point of view, the lower supply voltage leads the low power consumption. However, most of the specifications of the OTA rely strongly on the supply voltage. The performances

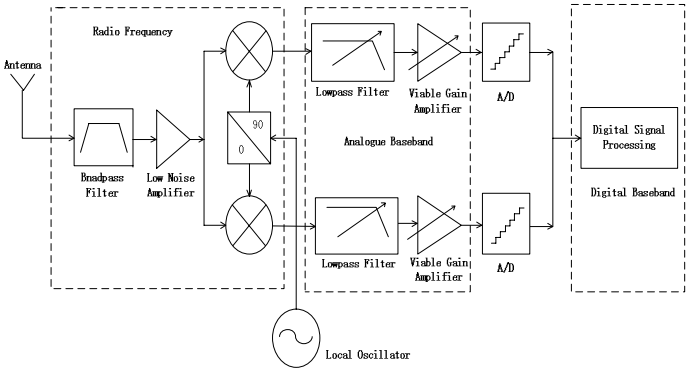

Figure 1 Receiver channels

of the OTA are decreased with the low supply voltage. Moreover, large transconductances are needed for the implementation of high-frequency filters. The implementation of large transconductances requires the use of wider transistors and large tail currents. The use of small transistor lengths pushes the parasitic poles to higher frequencies, but the OTA dc gain is reduced and mobility degradation effects become more severe. On the other hand, the use of large drain currents reduces even further the transistor dc gain and increases the power consumption. At the filter design point of view, the sensitivity and parasitic effects are important. The cascade method has been widely used for wireless communication and computer hard disk drive (HDD) design [4-6]. However, the cascade suffers from the relative high sensitivity, especially as filters order increasing. The LC ladder simulation method is insensitive, but the floating capacitors are needed, which is sensitive to the parasitic effects [7, 8]. Moreover, converting the passive components into OTA leads significant power consumption. The multiple loop feedback (MLF) based configurations are insensitive and can be used for very high frequency (VHF) as well as low power consumption applications [9, 10]. All the high impedance nodes are grounded with capacitors, thus the parasitic effects are minimum. Therefore, we proposed a fourth-order Gm-C lowpass filter based on leap-

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frog (LF) MLF configuration in this paper. The Nauta OTAs are used to implement the filter. The cut-off frequency of 240MHz with 22.3mW power consumption is achieved. Both of the filter and OTA are designed in standard TSMC 0.18µm process and the cut-off frequency of the filter can also be controlled in the range of 240-300MHz.

The design of a fully-balanced Nauta OTA is discussed in Section II. Filter architecture and synthesis are described in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. FULLY-BALANCED NAUTA OTA

The differential transconductance circuit described by Nauta [11] was selected for this filter. This circuit has advantages for high frequency designs using deep-submicron CMOS technology; there are no internal nodes to give rise to parasitic poles, the relatively high output conductance of sub-micron MOSFETs can be compensated by choosing transistor sizes appropriately, and large input and output voltage swings are possible for a given supply voltage. The transconductance of the Nauta OTA is dependant on the supply voltage V_{dd}, which provides a means of tuning the filter.

The basis of the Nauta OTA is a differential transconductor using two inverters, g1, and g2, as shown in Figure 2.

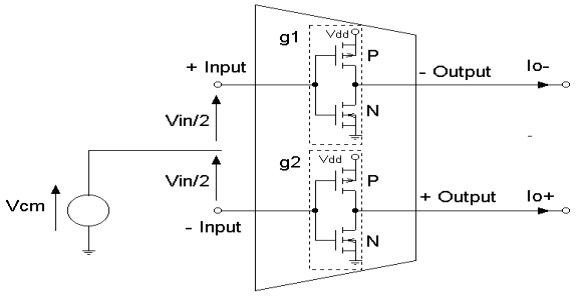

Figure 2 Differential transconductor using inverters

Assuming the P- and N-channel MOSFETs have ideal square law transfer functions can be expressed:

$$I_{dp} = \frac{K_p W_p}{L_p}\left(V_{gsp} - V_{tp}\right)^2, \qquad I_{dn} = \frac{K_n W_n}{L_n}\left(V_{gsn} - V_{tn}\right)^2, \tag{1}$$

where W_p, L_p, W_n, L_n are the widths and lengths of the P- and N- channel devices, and K_p, K_n are approximately $\mu C_{ox}/2$ for the P- and N- channel devices respectively, the transfer function of the transconductor can be calculated:

$$I_{o-} = \frac{K_p W_p}{L_p}\left(V_{dd} - V_{cm} - \frac{V_{in}}{2} - V_{tp}\right)^2 - \frac{K_n W_n}{L_n}\left(V_{cm} + \frac{V_{in}}{2} - V_{tn}\right)^2;$$

$$I_{o-} = \frac{K_p W_p}{L_p}\left(\begin{array}{l} V_{dd}^2 + V_{cm}^2 + \frac{V_{in}^2}{4} + V_{tp}^2 - 2V_{dd}V_{cm} - V_{dd}V_{in} \\ -2V_{dd}V_{tp} + V_{cm}V_{in} + 2V_{cm}V_{tp} + V_{in}V_{tp} \end{array}\right) - \frac{K_n W_n}{L_n}\left(V_{cm}^2 + \frac{V_{in}^2}{4} + V_{tn}^2 + V_{cm}V_{in} - 2V_{cm}V_{tn} - V_{in}V_{tn}\right) \tag{2}$$

Similarly, at the non-inverting output I_{o+}, with V_{in} replaced by $-V_{in}$. Both inverter outputs contain non-linear square-law terms. The differential output current is the difference between I_{o-} and I_{o+}:

$$I_o = I_{o+} - I_{o-} = \frac{K_p W_p}{L_p}\left(2V_{dd}V_{in} - 2V_{cm}V_{in} - 2V_{in}V_{tp}\right) - \frac{K_n W_n}{L_n}\left(-2V_{cm}V_{in} + 2V_{in}V_{tn}\right) \tag{3}$$

Thus all the non-linear terms cancel in the differential output current (I_{o+}-I_{o-}), being present only as equal common-mode components in I_{o+} and I_{o-}. The linearity of the differential transfer function is independent of matching between the P- and N-channel devices, provided both have a square law response. Since in practice the OTA will be used as an integrator with a capacitive load, it is necessary to set V_{cm} so that the output current is zero with zero differential input voltage, in order to avoid the capacitors charging. The value of V_{cm} at which I_{o+} and I_{o-} are zero is found by setting $I_{dn} = I_{dp}$:

$$V_{cm} = \frac{\sqrt{\frac{K_n W_n}{L_n} \Big/ \frac{K_p W_p}{L_p}}.V_{tn} + V_{dd} - V_{tp}}{1 + \sqrt{\frac{K_n W_n}{L_n} \Big/ \frac{K_p W_p}{L_p}}} \tag{4}$$

If a number of integrators using these OTAs are connected in a network with overall negative feedback, the quiescent operating point of the transconductors will then be V_{cm}. If $K_n W_n/L_n$ is made equal to $K_p W_p/L_p$, and $V_{tn} = V_{tp}$ (for normal CMOS processes the threshold voltages of the P- and N-channel devices are nominally equal), this reduces to $V_{cm} = V_{dd}/2$. This is desirable for a practical circuit, since with the quiescent operating point of the inverters set mid-way between the supply rails, the maximum symetrical output voltage swing is available. Assuming this condition is used in practice, putting these values into (3) and differentiating gives the small-signal transconductance:

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$$g_m = \frac{dI_o}{dV_{in}} = \frac{2V_{dd}K_nW_n}{L_n} = \frac{2V_{dd}K_pW_p}{L_p} \tag{5}$$

Transconductance g_m is thus proportional to supply voltage V_{dd}; clearly this is only true as long as the transistors remain in saturation, which limits the minimum supply voltage and transconductance which can be used; reducing the supply voltage also reduces the available input and output voltage swing. The two-inverter transconductor by itself has common-mode gain equal to the differential mode gain, i.e. common-mode rejection of 0dB. This is undesirable, since under large-signal conditions in a multi-stage filter, the common-mode square law distortion terms could sum together and become large. Additionally, especially for dep sub-micron geometry devices, the output resistance of the inverters is quite low, leading to low integrator DC gain, and correspondingly low Q. The addition of four more inverters g_{m3}-g_{m6} provides control of common-mode gain, and output resistance, as shown in the complete Nauta OTA circuit in Figure 3.

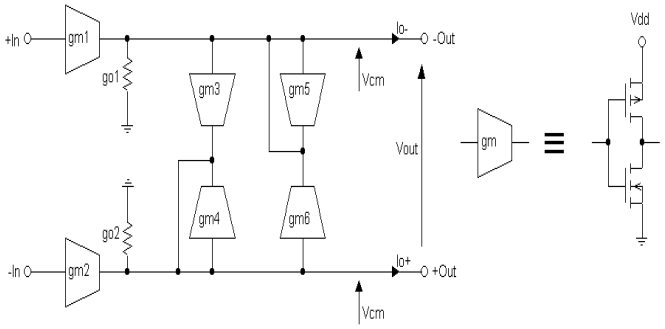

Figure 3 Full Nauta OTA circuit, with common-mode gain control

Considering the inverting output, with the input voltage set to zero and a differential output V_{out} present:

$$\begin{aligned} I_{o-} &= \frac{g_{o1}V_{out}}{2} + \frac{g_{m5}V_{out}}{2} - \frac{g_{m6}V_{out}}{2} \\ &= \frac{V_{out}}{2}\left(g_{o1} + g_{m5} - g_{m6}\right) \end{aligned} \tag{6}$$

Therefore if g_{m6} is made slightly larger so that $g_{m6} = g_{m5} + g_{o1}$, the output current will be zero, and the output resistance infinite. However, for a common-mode signal V_{cm} applied to both outputs is expressed in (7). So the output of g_1 is effectively loaded by a resistance $1/(g_{o1}+g_{m5}+g_{m6})$ for common-mode signals, while simultaneously for differential-mode signals the DC output resistance can be made infinite by suitable sizing of g_{m5} and g_{m6}. The same function is performed for the non-inverting output by g_{m3} and g_{m4}. Making $g_{m3} - g_{m6}$ larger results in lower common-mode gain, but greater power consumption, chip area and parasitic capacitance, and also requires better matching between transconductors. As a compromise, the area of $g_{m3} - g_{m6}$ was made approximately half that of g_{m1}, g_{m2}, yielding a common-mode gain of around unity. The widths of g_{m3} and g_{m6} were increased empirically, and the open-loop gain of the complete OTA plotted, to find the optimum sizes for maximizing the low frequency gain and therefore the output resistance.

$$\begin{aligned} &I_{o-} = g_{o1}V_{cm} + g_{m5}V_{cm} + g_{m6}V_{cm}, \\ &\therefore R_{out}\ (\text{for common mode signals}) = \frac{V_{cm}}{-I_{o-}} \\ &= \frac{1}{(g_{o1}+g_{m5}+g_{m6})} \end{aligned} \tag{7}$$

III. FILTER ARCHITECTURE AND SYNTHESIS

The fourth-order Butterworth approximation is chosen to implement the continuous-time lowpass filter in this section. The normalized characteristic of a fourth-order Butterworth lowpass filter at the cut-off frequency is given by:

$$H_d(s) = \frac{1}{s^4 + 2.61313s^3 + 3.41421s^2 + 2.61313s + 1} \tag{8}$$

The fully balanced realization of the function in (8) using the current-mode LF MLF configuration is shown in Figure 4.

The overall transfer function of the circuit can be derived as

$$H(s) = \frac{I_{output}}{I_{input}} = \frac{1}{D(s)} \tag{9}$$

where

$$D(s) = \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_3\tau_4)s^2 + (\tau_2 + \tau_4)s + 1$$

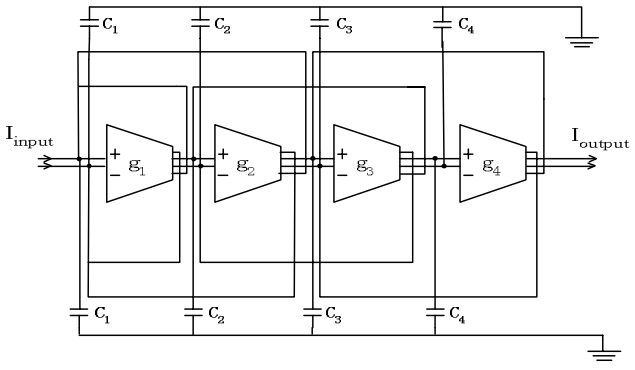

Figure 4 Butterworth fourth–order current-mode LF MLF Gm–C filter network

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The design formulae for the filter can be attained by coefficient matching between (8) and (9) [12]. The resulting pole $\tau_i=C_i/g_i$ parameters are:

$$\tau_1 = 0.3827, \tau_2 = 1.0824, \tau_3 = 1.5772, \tau_4 = 1.5307 \quad (10)$$

The filter is designed with identical unit OTAs using the CMOS OTA cell in Figure 3 to improve OTA matching and facilitate design automation. The cut-off frequency of the filter is chosen around 240 MHz. Using the computed parameter values in (10) and choosing identical transconductance of 1.5mS for g_i (i=1,2…4) the capacitor values can be calculated, but the parasitic capacitance must also be taken into account. For the circuit of Figure 3, the parasitic capacitance is about 0.1pF. The capacitance values are recalculated below:

C_1=0.6612pF, C_2=2.0534pF, C_3=3.0378pF, C_4=2.9452pF.

IV. SIMULATION RESULTS

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18µm CMOS process available from MOSIS [13]. Figure 5 shows the magnitude response of the filter with differential supply voltage. As can be seen from Figure 5, by varying the supply voltage of the unit OTA cell, the tuning range of cut–off frequency is around 240–300MHz. The maximum total power consumption of the filter is about 55mW at 300MHz of cut-off frequency and the minimum total power consumption of the filter is about only 22.3mW at 240MHz of cut-off frequency for a single 1.5V power supply. Simulation of the filter has also shown a total harmonic distortion (THD) of less than 1% with a single tone of 750µA. The dynamic range is about 58dB at f_c =240MHz. The performance of the filter offers significant improvements; especially the power consumption is smaller than other designs in the literature, making the presented filter well suitable for portable electronics products.

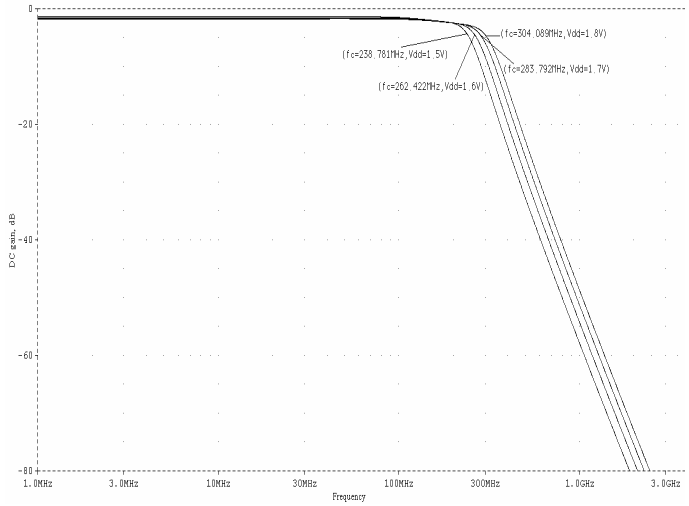

Figure 5 Simulated magnitude response of the filter with different bias voltage

V. CONCLUSIONS

This paper has described a 240MHz current-mode fully-balanced fourth-order Butterworth lowpass filter based on the LF MLF configuration, applied to the UWB applications. A linear single stage Nauta OTA with a typically large transconductance has been used. Simulation results using 1.5V 0.18µm CMOS show that the power consumption of proposed filter is about 22.3mW at f_c = 240MHz. The frequency tuning range is from 240MHz to 300MHz. These results have shown that the current-mode MLF LF filter can achieve very high frequency with relatively low power consumption and may become one of the filtering solutions for future UWB systems.

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