EFFICIENT MODELING AND ANALYSIS OF CLOCK FEED-THROUGH AND CHARGE INJECTION OF SWITCHED CURRENT CIRCUITS

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ABSTRACT

This paper presents an efficient modeling and frequency domain analysis method for analyzing the effect of the clock feed-through and charge injection in switched current circuits. The effect of clock feed-through is analyzed by modeling the clock signal using two constant voltage sources that are switched periodically. The charge injection is depicted using two impulse charge sources that inject charge into both the source and drain terminals of MOS switches when the devices undergo a ON-to-OFF transition. In addition, both parasitic capacitances and channel resistance of MOS switches are considered. The analysis is carried out using the approach for periodically switched linear circuits. A computer program has been developed. Simulation results on example circuits are presented.

1. INTRODUCTION

Switched-current circuits that emerged in late 1980s possess many intrinsic advantages over switched capacitor counterparts in low supply voltage, wide dynamic range, high bandwidth, and full compatibleness with standard digital CMOS technology [1]. The effectiveness of these circuits, however, is undermined by the effect of the non-idealities of these circuits. Among them, clock feed-through (CFT) and charge injection are predominant. Clock feed-through and charge injection deteriorate the performance of switched-current circuits mainly because of the comparable value of the load capacitance and that of gate capacitance, including overlap capacitance, of MOS switches. Efficient and accurate analysis of these effects is vital, especifically for circuits implemented using deep sub-micron CMOS technology. An analytical analysis of the effect of CFT and charge injection was carried out in [2, 3]. Theses models, though accurate, are often too complex to be used for efficient computer analysis. In [4], a z-domain approach was proposed for analysis of switched current filters. Switches are modeled as an ideal OPEN/CLOSED switch depending upon the state of the clock. Neither clock feed-through nor charge injection can be analyzed. The computer analysis method for switched current circuits in [5] takes into account both parasitic capacitances and resistances in the circuits, it, however, can not analyze the effect of clock feed-through, nor the effect of charge injection. In this paper, an accurate mode and an efficient analysis method for analysis of the effect of charge injection, CFT, and all the parasitic capacitances of MOS transistors are proposed. The charge injected to both the source and drain during the turn-off transition of MOS switches is represented by impulsive charge sources. The effect of clock feed-though is analyzed by considering both intrinsic capacitance and parasitic capacitances of MOS switches.

2. MODELING OF CLOCK FEED-THROUGH AND CHARGE INJECTION

Clock feed-through affects the performance of switched current circuits via the intrinsic capacitances and parasitic overlapping capacitances between the gate and the source/drain. Clock feed-through is not of critical concern in switched-capacitor networks mainly because the capacitance of the linear sampling capacitors is usually much larger than that of the coupling capacitances between the gate and source/drain of MOS switches. Switched current circuits differ from switched capacitor counterparts by excluding linear capacitors. Data sampling and storage are performed by the capacitances of MOS transistors. In this case, the capacitance of coupling capacitors becomes comparable to that of storage capacitors, especially for deep sub-micron technology. To efficiently model the effect of clock feed-through, in this paper the clock signal applied to the gate of MOS

switches is represented by two constant voltage sources V_{OL} and V_{OH} that are sampled periodically as shown in Fig.1, where V_{OH} and V_{OL} represent the HIGH and LOW of the clock signal respectively.

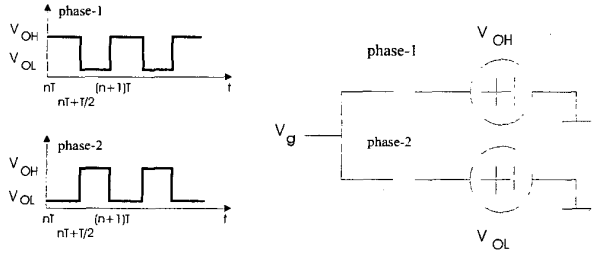

Figure 1: A Model of a 2-phase 50% duty cycle clock

In addition to the clock feed through, switched current circuits are also subject to the effect of charge injection. Most of the charge stored in the channel of a ON-state MOS switch will be injected into both the drain and source of the switch when the gate voltage is removed. Depending upon the impedance seen by the drain and source, the amount of charge injected to the source and drain differ, as shown in [3]. Although physically the charge removal process is initiated when the gate voltage starts to drop, for efficient modeling and analysis, it is assumed that the charge stored in the channel is removed instantaneously when the device undergoes a transition from the strong inversion to cutoff modes. A Dirac function can therefore be employed to model this transition. By assuming that MOS switches are biased in the triode region when they are in the ON-state and the charge stored in the channel is slipped evenly between the source and drain when it enters the ON-to-OFF transition, the charge injected into the source and drain can therefore be modeled using two impulse charge sources as follows

$$q(t) = \sum_{n=-\infty}^{\infty} \frac{1}{2} C'_{ox} W L \delta(t - nT - \frac{T}{2}), \qquad (1)$$

where C'_{ox} is the gate-to-channel capacitance per unit area, W and L are width and length of the MOS switch, respectively.

3. ANALYSIS OF CLOCK FEED-THROUGH AND CHARGE INJECTION IN FREQUENCY DOMAIN

When only considering linear characteristics, switched current circuits can be analyzed effectively using the method for periodically switched linear circuit [6]. To demonstrate how the effect of both the clock feed-through and charge injection of switched current circuit is analyzed, a test circuit shown in Fig.2 is employed. The equivalent circuit of the test circuit is given in Fig.3 when the clock is in phase 1 and Fig.4 when the clock is in phase 2. Note that G_{on} is the channel conductance when the device is in the triode region, C_s and G_s are respectively the capacitance and conductance of the matching network, C_L is the load capacitance, C_{gs} and C_{gd} are the gate-source and gate-drain capacitances respectively, C_{sb} and C_{db} are the source-substrate and drain-substrate capacitances respectively, and C_{ov} is the overlap capacitance. The charge sources inject charge to the source and drain at the time instant $t = nT + \frac{T}{2}$ when the switch undergoes a ON-to-OFF transition. These charge sources are incorporated into the circuit equation as the initial conditions of phase 2. Note that in phase 2, both the gate-source and gate-drain capacitances vanish.

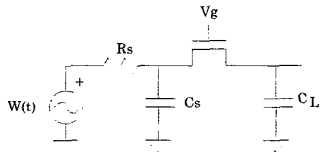

Figure 2: Test circuit

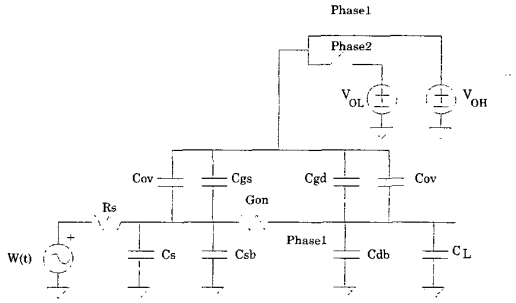

Figure 3: Equivalent circuit of the test circuit in phase 1

The clock with multiple phases is shown in Fig.5. The input of the circuit is given by $w(t) = A\sin(\omega_o t)$, where A is the amplitude and ω_o is the frequency. Using modified nodal analysis (MNA) the circuit is represented by

$$\mathbf{G}_k \mathbf{v}_k(t) + \mathbf{C}_k \frac{d\mathbf{v}_k(t)}{dt}$$

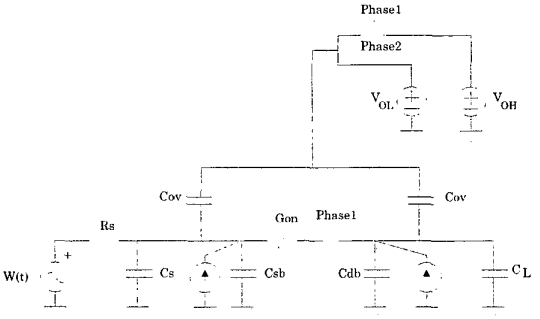

Figure 4: Equivalent circuit of the test circuit in phase 2

$$
\begin{aligned}
&= \mathbf{g}_1\xi_k(t)\frac{Ae^{j\omega_o t}}{2j} - \mathbf{g}_2\xi_k(t)\frac{Ae^{-j\omega_o t}}{2j} \\
&+ \mathbf{g}_3\xi_k(t)V_{OH} + \mathbf{g}_4\xi_k(t)V_{OL} \\
&+ \mathbf{C}_{k-1}\mathbf{v}_{k-1}(nT+\sigma_{k-1})\delta(t-nT-\sigma_{k-1}) \\
&- \mathbf{C}_k\mathbf{v}_k(nT+\sigma_k)\delta(t-nT-\sigma_k) \\
&\quad k=1,2 \qquad (2)
\end{aligned}
$$

where $\mathbf{v}_k(t)$ is the network variable vector in phase k. $\mathbf{G}_k$ and $\mathbf{C}_k$ are the conductance and capacitance matrices in phase k. $\mathbf{g}_1$, $\mathbf{g}_1, \mathbf{g}_3$, and $\mathbf{g}_4$ are constant vectors specifying the connection of the inputs $\frac{e^{j\omega_o t}}{2j}$, $\frac{e^{-j\omega_o t}}{-2j}, V_{OH}$, and V_{OL} respectively, $\xi_k(t)$ is the k-th window function defined as : $\xi_k(t) = 1$ if $nT+\sigma_{k-1} < t \leq nT+\sigma_k$ and 0, elsewhere. Note that using Euler identity $\sin(\omega_o t) = (e^{j\omega_o t} - e^{-j\omega_o t})/(2j)$, the sinusoidal input is represented by two exponential inputs. The first Dirac delta term at $t = nT+\sigma_{k-1}$ represents the effect of the initial conditions, whereas the second Dirac term at $t = nT+\sigma_k$ represents the extraction of the final conditions to ensure the the contribution of circuit in phase k to the output vanishes outside the phase.

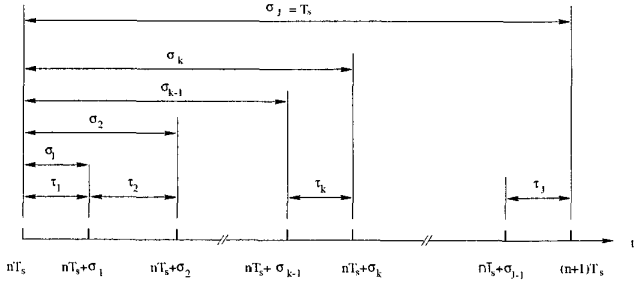

Figure 5: Clock with multiple phases

The frequency response $\mathbf{V}_k(j\omega)$ is obtained by applying Fourier transform to (2)

$$
\begin{aligned}
&(\mathbf{G}_k + j\omega\mathbf{C}_k)\mathbf{V}_k(j\omega) \\
&= \frac{A}{2j}\mathbf{g}_1\mathcal{F}[\xi_k(t)e^{j\omega_o t}] - \frac{A}{2j}\mathbf{g}_2\mathcal{F}[\xi_k(t)e^{-j\omega_o t}] \\
&+ \mathbf{g}_3V_{OH}\mathcal{F}[\xi_k(t)] + \mathbf{g}_4V_{OL}\mathcal{F}[\xi_k(t)] \\
&+ \mathbf{C}_{k-1}\mathcal{F}[\mathbf{v}_{k-1}(nT+\sigma_{k-1})\delta(t-nT-\sigma_{k-1})] \\
&- \mathbf{C}_k\mathcal{F}[\mathbf{v}_k(nT+\sigma_k)\delta(t-nT-\sigma_k)] \qquad (3)
\end{aligned}
$$

where $\mathcal{F}[.]$ is the Fourier transform operator. Because

$$
\begin{aligned}
\mathcal{F}[e^{j\omega_o t}\xi_k(t)] &= 2\pi\sum_{n=-\infty}^{\infty}\theta_{k,n}\delta(\omega-\omega_o-n\omega_s), \\
\mathcal{F}[e^{-j\omega_o t}\xi_k(t)] &= 2\pi\sum_{n=-\infty}^{\infty}\theta_{k,n}\delta(\omega+\omega_o-n\omega_s), \\
\mathcal{F}[\xi_k(t)] &= 2\pi\sum_{n=-\infty}^{\infty}\theta_{k,n}\delta(\omega-n\omega_s),
\end{aligned}
$$

and

$$
\theta_{k,n} = \begin{cases} \frac{\tau_k}{T} & n=0 \\ e^{-jn\omega_s\sigma_{k-1}}\frac{1-e^{-jn\omega_s\tau_k}}{jn\omega_s T} & \text{otherwise} \end{cases},
$$

where $\omega_s = 2\pi/T$, the frequency domain response $\mathbf{V}_k(j\omega)$ is obtained once the quantities $\mathcal{F}[\mathbf{v}_{k-1}(nT+\sigma_{k-1})\delta(t-nT-\sigma_{k-1})]$ and $\mathcal{F}[\mathbf{v}_k(nT+\sigma_k)\delta(t-nT-\sigma_k)]$ are available. To simplify analysis, let the number of phases in a clock period be 2 and the duty cycle of the clock be 50% so that the durations of ON and OFF states are $\frac{T}{2}$. To obtain these two quantities we notice that in phase 1 where $t \in [nT, nT+\frac{T}{2})$ the time origin is at $t = nT$, and the two exponential inputs are $\frac{A}{2j}e^{j\omega_o nT}e^{j\omega_o t}$ and $\frac{A}{-2j}e^{-j\omega_o nT}e^{-j\omega_o t}$. The circuit in this phase is essentially linear time-invariant and is represented by

$$
\begin{aligned}
&\mathbf{G}_1\mathbf{v}_1(t) + \mathbf{C}_1\frac{d\mathbf{v}_1(t)}{dt} \\
&= \mathbf{g}_1\frac{A}{2j}e^{j\omega_o nT}e^{j\omega_o t} - \mathbf{g}_2\frac{A}{2j}e^{-j\omega_o nT}e^{-j\omega_o t} \\
&+ \mathbf{g}_3V_{OH}u(t) \qquad (4)
\end{aligned}
$$

with the initial condition given by $\mathbf{v}_1(0^-) = \mathbf{v}_2(nT)$. Taking Laplace transform and then its inverse, we obtain the response of the circuit at the end of phase 1

$$
\mathbf{v}_1(nT+\frac{T}{2}) = \mathbf{M}_1\mathbf{v}_2(nT)
$$

$$+ \quad \frac{A}{2j}e^{j\omega_o nT}\mathbf{P}_{11} - \frac{A}{2j}e^{-j\omega_o nT}\mathbf{P}_{21} + V_{OH}\mathbf{A}_1\mathbf{g}_3 \tag{5}$$

where

$$\mathbf{M}_1 = \mathcal{L}^{-1}\Big[(\mathbf{G}_1 + s\mathbf{C}_1)^{-1}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{P}_{11} = \mathcal{L}^{-1}\Big[(\mathbf{G}_1 + s\mathbf{C}_1)^{-1}\frac{\mathbf{g}_1}{s-j\omega_o}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{P}_{21} = \mathcal{L}^{-1}\Big[(\mathbf{G}_1 + s\mathbf{C}_1)^{-1}\frac{\mathbf{g}_2}{s+j\omega_o}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{A}_1 = \mathcal{L}^{-1}\Big[(\mathbf{G}_1 + s\mathbf{C}_1)^{-1}\frac{1}{s}\Big]_{t=\frac{T}{2}}, \tag{6}$$

and $\mathcal{L}^{-1}[.]$ is inverse Laplace transform operator. Seen from the above development is that $\mathbf{M}_1$ is the transition matrix of the circuit in phase 1, $\mathbf{P}_{11}, \mathbf{P}_{21}$, and $\mathbf{A}_1$ are the zero-state responses of the circuit in phase 1 to the inputs $\frac{A}{2j}e^{j\omega_o t}$, $-\frac{A}{2j}e^{-j\omega_o t}$, and V_{OH} respectively.

In phase 2 where $t \in [nT + \frac{T}{2}, nT + T)$, the origin of time is shifted from $t = nT$ to $t = nT + \frac{T}{2}$. Subsequently, the two inputs become $\frac{A}{2j}e^{j\omega_o(nT+\frac{T}{2})}e^{j\omega_o t}$ and $\frac{A}{-2j}e^{-j\omega_o(nT+\frac{T}{2})}e^{-j\omega_o t}$, and the circuit is depicted by

$$\mathbf{G}_2\mathbf{v}_2(t) + \mathbf{C}_2\frac{d\mathbf{v}_2(t)}{dt} = \frac{A}{2j}\mathbf{g}_1 e^{j\omega_o(nT+\frac{T}{2})}e^{j\omega_o t} - \frac{A}{2j}\mathbf{g}_2 e^{-j\omega_o(nT+\frac{T}{2})}e^{-j\omega_o t} + \mathbf{g}_4 V_{OL}u(t) \tag{7}$$

with the initial condition given by $\mathbf{v}_2(0^-) = \mathbf{v}_1(nT + \frac{T}{2})$. Following the similar approach as that for phase 1, we arrive at

$$\mathbf{v}_2(nT+T) = \mathbf{M}_2\mathbf{v}_1(nT+\frac{T}{2}) + \frac{A}{2j}e^{j\omega_o(nT+\frac{T}{2})}\mathbf{P}_{12} - \frac{A}{2j}e^{-j\omega_o(nT+\frac{T}{2})}\mathbf{P}_{22} + V_{OL}\mathbf{A}_2\mathbf{g}_4 \tag{8}$$

where

$$\mathbf{M}_2 = \mathcal{L}^{-1}\Big[(\mathbf{G}_2 + s\mathbf{C}_2)^{-1}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{P}_{12} = \mathcal{L}^{-1}\Big[(\mathbf{G}_2 + s\mathbf{C}_2)^{-1}\frac{\mathbf{g}_1}{s-j\omega_o}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{P}_{22} = \mathcal{L}^{-1}\Big[(\mathbf{G}_2 + s\mathbf{C}_2)^{-1}\frac{\mathbf{g}_2}{s+j\omega_o}\Big]_{t=\frac{T}{2}},$$
$$\mathbf{A}_2 = \mathcal{L}^{-1}\Big[(\mathbf{G}_2 + s\mathbf{C}_2)^{-1}\frac{1}{s}\Big]_{t=\frac{T}{2}}.$$

Applying Fourier transform to (5) and (8) and noting that

$$\mathcal{F}\Big[e^{j\omega_o(nT+\frac{T}{2})}\Big] = e^{j\omega_o\frac{T}{2}}\frac{2\pi}{T}\sum_{n=-\infty}^{\infty}\delta(\omega - \omega_o - n\omega_s)$$
$$\mathcal{F}\Big[\mathbf{v}_1(nT+\frac{T}{2})\Big] = e^{j\omega\frac{T}{2}}\mathbf{V}_1(j\omega)$$
$$\mathcal{F}\Big[\mathbf{v}_2(nT+T)\Big] = e^{j\omega T}\mathbf{V}_2(j\omega)$$

we have

$$e^{j\omega\frac{T}{2}}\mathbf{V}_1(j\omega) = \mathbf{M}_1\mathbf{V}_2(j\omega) + \frac{A}{2j}\frac{2\pi}{T}\mathbf{P}_{11} - \frac{A}{2j}\frac{2\pi}{T}\mathbf{P}_{21} + V_{OH}\mathbf{g}_3\mathbf{A}_1\frac{1}{j\omega} \tag{9}$$

$$e^{j\omega T}\mathbf{V}_2(j\omega) = \mathbf{M}_2 e^{j\omega\frac{T}{2}}\mathbf{V}_1(j\omega) + \frac{A}{2j}e^{j\omega_o\frac{T}{2}}\frac{2\pi}{T}\mathbf{P}_{12} - \frac{A}{2j}e^{-j\omega_o\frac{T}{2}}\frac{2\pi}{T}\mathbf{P}_{22} + V_{OL}\mathbf{g}_4\mathbf{A}_2\frac{1}{j\omega} \tag{10}$$

Writing the above two equations in matrix format gives

$$\begin{bmatrix} e^{j\omega\frac{T}{2}}\mathbf{I} & -\mathbf{M}_1 \\ -\mathbf{M}_2 e^{j\omega\frac{T}{2}} & e^{j\omega T}\mathbf{I} \end{bmatrix}\begin{bmatrix} \mathbf{V}_1(j\omega) \\ \mathbf{V}_2(j\omega) \end{bmatrix} = \frac{A\pi}{jT}\begin{bmatrix} \mathbf{P}_{11} \\ \mathbf{P}_{12}e^{j\omega_o\frac{T}{2}} \end{bmatrix} - \frac{A\pi}{jT}\begin{bmatrix} \mathbf{P}_{21} \\ \mathbf{P}_{22}e^{-j\omega_o\frac{T}{2}} \end{bmatrix} + \frac{1}{j\omega}\begin{bmatrix} V_{OH}\mathbf{A}_1\mathbf{g}_3 \\ V_{OL}\mathbf{A}_2\mathbf{g}_4 \end{bmatrix} \tag{11}$$

where $\mathbf{I}$ is a identity matrix of appropriate dimensions. It should be noted that the above equation is valid for $\omega = \omega_o + n\omega_s$, $n = 0, \pm1, \pm2, ...$ The complete frequency domain response can therefore be obtained by substituting (11) into (3).

4. EXAMPLES

The above presented method has been implemented in a computer program. The test circuit presented earlier is solved and the results are presented. The element values of the test circuit in simulation are as follows : $G_s = 1/50$ S, $g_{ON} = 0.303\times10^{-3}$ S,$C_s =$

1×10^{-12}F, $C_{sb} = C_{db} = 0.815\times10^{-12}$ F, $C_{gs} = C_{gd} = 8.17\times10^{-12}$F, $C_{ov} = 2.06\times10^{-12}$F, $C_L = 20\times10^{-12}$F, V_{OH} = 3.3V, and V_{OL} = 0V. The clock frequency is set to 10 MHz with 50 % duty cycle. The amplitude of the input sinusoidal is set to 1 mV (-60 dB). The voltage across the load capacitor C_L is computed using the method presented in the paper and the results are plotted in Fig. 6. As can be seen that the response decreases with the increase in frequency. To investigate the effect of clock feed-through, we double the value of the overlapping capacitance. The corresponding response is shown in Fig.7 with the solid line representing the response before C_{ov} is increased and the broken line the response after C_{ov} is doubled. It is seen that with the increase in the overlapping capacitances the voltage of the load capacitance increases, indicating that clock feed through increases the response of the circuit. Similarly by increasing the load capacitance, the effect of the clock feed through will be reduced. Subsequently the voltage across the load capacitor will be reduced. This is indeed true as shown in Fig.8. with the solid line representing the response before C_L is increased and the broken line the response after C_L is doubled.

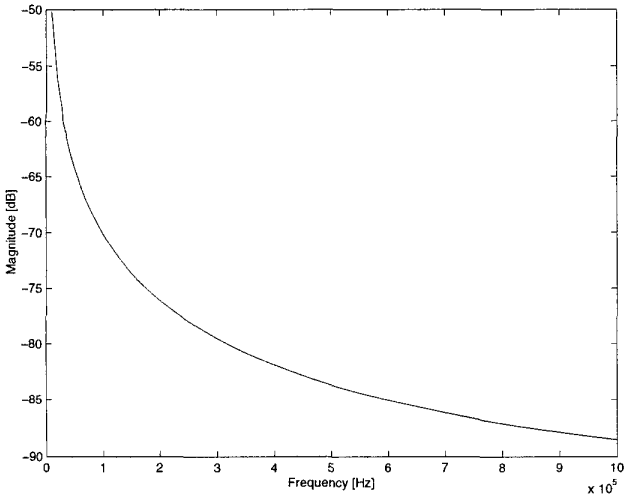

Figure 6: Voltage across the load capacitor

5. CONCLUSION

An efficient efficient modeling and frequency domain analysis method for analyzing the effect of the clock feed-through and charge injection in switched current circuits have been presented. The effect of clock feed-through is analyzed by modeling the clock signal using two constant voltage sources that are switched periodically. The charge injection is depicted using two

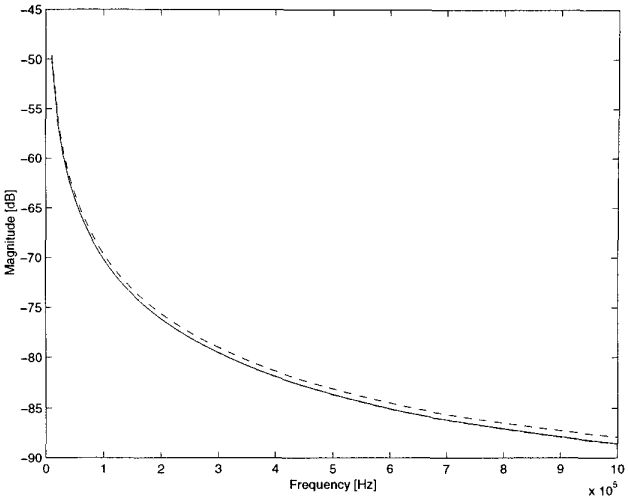

Figure 7: Voltage across the load capacitor with C_{ov} doubled

impulse charge sources that inject charge into both the source and drain terminals of MOS switches when the devices undergo a ON-to-OFF transition. The effect of clock feed through and charge injection can clearly be seen from simulation results. The method presented in this paper is completely general and applicable to linear switched circuits, including switched current and switched capacitor networks.

6. REFERENCES

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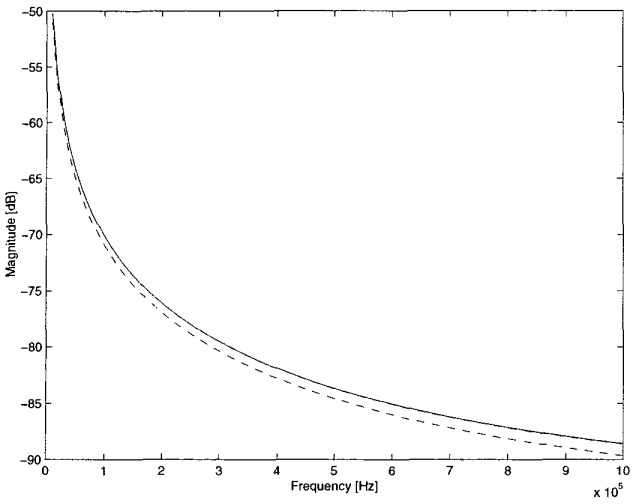

Figure 8: Voltage across the load capacitor with C_L doubled

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7. APPENDIX A

In this appendix we give an efficient algorithm for computing **A**. The algorithm is based on numerical inversion of Laplace transform, a numerical integration method that yields very accurate results [6]. Consider the circuit

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{g}u(t), \qquad \mathbf{v}(0^-) = \mathbf{0}, \quad (12)$$

where **g** is a constant vector specifying the nodes to which the input is connected. Its time-domain response at $t = \frac{T}{2}$ is obtained by first taking Laplace transform and then its inverse

$$\mathbf{v}(\frac{T}{2}) = \mathcal{L}^{-1}\left[(\mathbf{G} + s\mathbf{C})^{-1}\frac{1}{s}\right]_{t=\frac{T}{2}} \mathbf{g} = \mathbf{A}\mathbf{g}. \quad (13)$$

The above results indicate that if $\mathbf{g} = [1\ 0\ ...\ 0]^T$, where the superposition T denotes matrix transpose, then the response of the circuit gives the first column of **A**. By changing the position of the only nonzero entry in **g**, we can obtain other columns of **A**. In the following development we give a stepping algorithm to compute the first column of **A**. Other columns can be obtained in a similar manner. To avoid large errors due to a large step size $\frac{T}{2}$, the interval $\frac{T}{2}$ is divided into L subintervals of equal width $h = \frac{T}{2L}$. At $t \in [0, h)$, the circuit is depicted by (12). Its response at $t = h$ is given by

$$\mathbf{v}(h) = \mathcal{L}^{-1}\left[(\mathbf{G} + s\mathbf{C})^{-1}\frac{1}{s}\right]_{t=h} \mathbf{g} = \mathbf{A}(h)\mathbf{g}, \quad (14)$$

In the second step where $t \in [h, 2h)$, we set the time origin to $t = h$. As a result, the circuit is represented by

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{g}u(t), \qquad \mathbf{v}(0^-) = \mathbf{v}(h). \quad (15)$$

Its response at $t = h$ gives $\mathbf{v}(2h)$

$$\mathbf{v}(2h) = \mathbf{M}(h)\mathbf{v}(h) + \mathbf{A}(h)\mathbf{g}, \quad (16)$$

where $\mathbf{M}(h) = \mathbf{N}(h)\mathbf{C}$ and $\mathbf{N}(h) = \mathcal{L}^{-1}[\mathbf{G} + s\mathbf{C}]_{t=h}$. Continuing this process we obtain

$$\mathbf{v}[(n+1)h] = \mathbf{M}(h)\mathbf{v}(nh) + \mathbf{A}(h)\mathbf{g}. \quad (17)$$

Because $\mathbf{M}(h)$ and $\mathbf{A}(h)$ are constant for a fixed h, only matrix-vector multiplication and vector addition are needed. The algorithm yields the first column of $\mathbf{A}(\frac{T}{2})$ efficiently.

The computational efficiency of the algorithm, however, is undermined if the dimensions of $\mathbf{A}(\frac{T}{2})$ are large. A detail examination shows better computational efficiency can be achieved if we compute the complete matrix, rather than just a column $\mathbf{A}(\frac{T}{2})$. Using (13), the first, second, ..., mth columns of **A**, denoted respectively by $\mathbf{A}_1(2h), \mathbf{A}_2(2h), ..., \mathbf{A}_m(2h)$, are computed from $\mathbf{A}_1(2h) = \mathbf{M}(h)\mathbf{A}_1(h) + \mathbf{A}(h)\mathbf{g}_1$, $\mathbf{A}_2(2h) = \mathbf{M}(h)\mathbf{A}_2(h) + \mathbf{A}(h)\mathbf{g}_2$, ..., $\mathbf{A}_m(2h) = \mathbf{M}(h)\mathbf{A}_m(h) + \mathbf{A}(h)\mathbf{g}_m$, where $\mathbf{g}_m$ is a constant vector whose only nonzero entry is unity and is located at the mth position. Because $[\mathbf{g}_1\ \mathbf{g}_2\ ...\ \mathbf{g}_m] = \mathbf{I}$, where **I** is an identity matrix of appropriate dimensions, we obtain

$$\mathbf{A}(2h) = \mathbf{M}(h)\mathbf{A}(h) + \mathbf{A}(h). \quad (18)$$

Continuing this process we obtain

$$\mathbf{A}[(n+1)h] = \mathbf{M}(h)\mathbf{A}(nh) + \mathbf{A}(h). \quad (19)$$