# A Dual GTO Current Source Converter Topology with Sinusoidal Inputs for High Power Applications

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**Abstract:** A dual GTO current source converter topology with sinusoidal inputs is proposed for high power applications. The sinusoidal input current is realized by using PWM techniques to eliminate 11th and 13th harmonics and a transformer to cancel 5th, 7th, 17th and 19th harmonics. Three switching patterns are proposed with a switching frequency of 360Hz or 420Hz. The combination of these switching patterns provides a full range control over the dc output current. Resonant modes of the proposed system are identified and the criterion for the line capacitor design is provided. Simulation and experimental results are given to verify the theoretical analysis.

## I. Introduction

In high power (up to 10,000hp) ac motor drives using GTO current source inverter technology, SCR rectifiers are often used as a front end converter[1,2]. The SCR rectifier has the features of simple structure, reliable operation and bidirectional power flow. However, it injects harmonic currents into the power systems and its power factor is poor under light load conditions. A possible solution to these problems is to replace the SCR rectifier with a GTO PWM current source converter[3]. Figure 1 shows a simplified circuit diagram of a GTO ac/dc current source converter which can be used to replace SCR rectifier in high power induction motor drivers. Typically, the GTO devices are required to be connected in series in medium voltage (4160V to 6900V) applications.

For the design of high power GTO current source converter, one of the most important issues is the switching frequency, which should be kept as low as possible to minimize GTO switching and snubber power loss. This requirement is also imposed by the switching characteristics of high power GTO devices[4,5].

In order to minimize the switching frequency while keep input current close to sinusoidal, a novel GTO current source
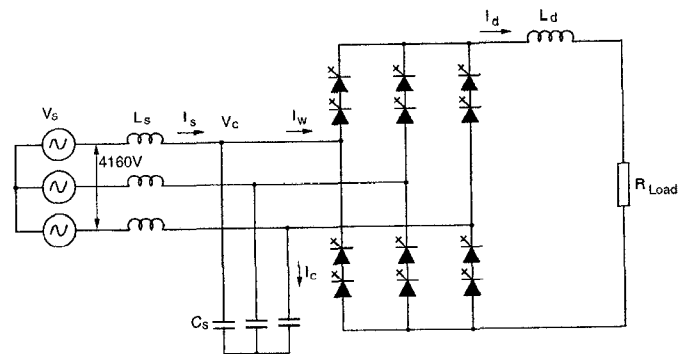


Fig.1   Circuit diagram of a high power GTO current source converter
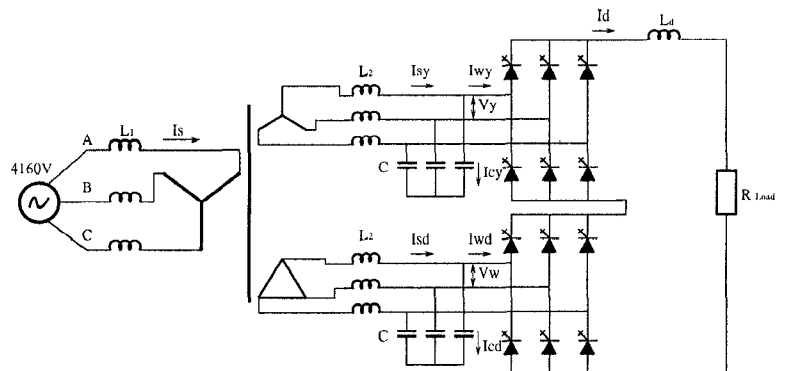


Fig. 2   A dual GTO PWM current source converter configuration

converter topology as shown in Fig. 2 is proposed. This topology is composed of two identical converters and an isolation transformer. The transformer is used to cancel certain harmonics produced by the converters. The other low order harmonics that cannot be cancelled by the transformer

are eliminated by PWM switching patterns. Compared with the single converter topology, the proposed dual converter has the following potential features:

- Sinusoidal input current. The transformer is used to cancel 5th, 7th, 17th and 19th harmonic currents while the PWM technique is employed to eliminate 11th and 13th harmonics. As a result, the input line current $I_s$ does not contain any harmonics whose order is lower than 23rd. The other high order harmonics can be easily filtered out by the line capacitor;

- Low switching frequency. As mentioned above, only 11th and 13th harmonics are required to be eliminated by the PWM pattern. Therefore, the lowest switching frequency for the proposed topology could be 360Hz. For the single converter to eliminate all the harmonics with the order lower than 23rd, the minimum switching frequency is 840Hz, which is too high to be implemented for high power applications; and

- Reliable operation for high voltage applications. No GTO devices are connected in series in the proposed topology. The dynamic/steady-state voltage sharing problem for the series devices in a single converter topology is completely avoided. The number of GTO devices for the dual converter topology mains the same as that for the single converter topology. For example, in a drive system with a supply voltage of 4160V, twelve 6000V GTO devices are required for both single and dual converter topologies. This concept can be easily used to develop a triple converter topology for higher voltage applications.

Compared with the single converter, the proposed topology requires a transformer, which may not be considered as a disadvantage. For example, in retrofit or new applications where a standard (off-the-shelf) ac motor is used, an isolation transformer between the utility supply and front-end converter is indispensable to eliminate excessive line-to-ground and neutral-to-ground voltage stress generated by the current source drives[6]. The transformer used in the dual converter topology serves the same purpose in addition to the harmonic cancellation. Therefore, the proposed topology is particularly suitable for this type of applications.

## II. Harmonic Cancellation

It is assumed that two sets of the transformer secondary windings are connected with a 30° phase shift. It can be proved that regardless of the current waveforms in the secondary windings, the 5th, 7th, 17th, 19th, 27th and 29th harmonic currents in these windings will be cancelled and do not appear in the primary windings.
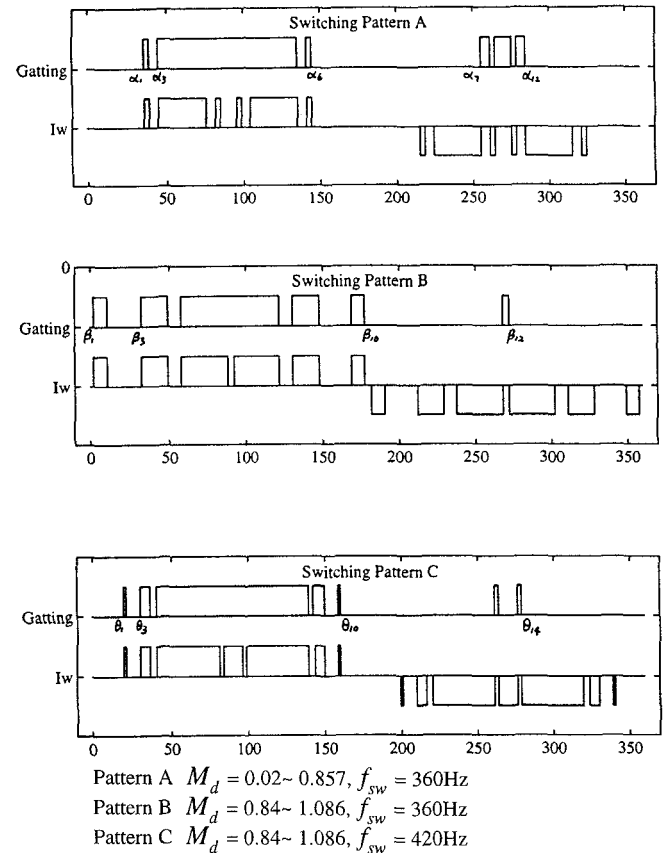


Pattern A  $M_d = 0.02 \sim 0.857$, $f_{sw} = 360$Hz
Pattern B  $M_d = 0.84 \sim 1.086$, $f_{sw} = 360$Hz
Pattern C  $M_d = 0.84 \sim 1.086$, $f_{sw} = 420$Hz

Fig. 3    Three proposed switching pattern

## III. Switching Patterns

The basic requirements for the design of switching patterns for the proposed topology are as follows:

- To eliminate 11th and 13th harmonics;
- To provide an adjustable dc current over a full range by adjusting modulation index;
- To minimize switching frequency.

Besides these requirements, the switching pattern design must satisfy a constraint, that is, only one switching device in the upper legs of the converter and one in the lower legs can be turned on at any time to guarantee a continuous dc output current and a defined converter input current.

Figure 3 shows three switching patterns developed for the dual converter topology. Pattern A and B have a switching frequency of 360HZ, which is the lowest possible frequency to satisfy the first two requirements. Pattern C has a switching frequency of 420Hz. Figure 4 illustrates the calculated switching angles for the Switching Patterns A and B, which can be used in a modulation index range of 0.02 to 0.857 and 0.84 to 1.085, respectively. As shown in Fig. 4, some of the angles will approach to a same value when the modulation index increases from zero to 0.857 ( e.g., $\alpha_9$ and $\alpha_{10}$ ) or decreases for 1.085 to 0.84 ( such as $\beta_3$ and $\beta_4$ ). When these angles are merged, the 11th and 13th harmonics
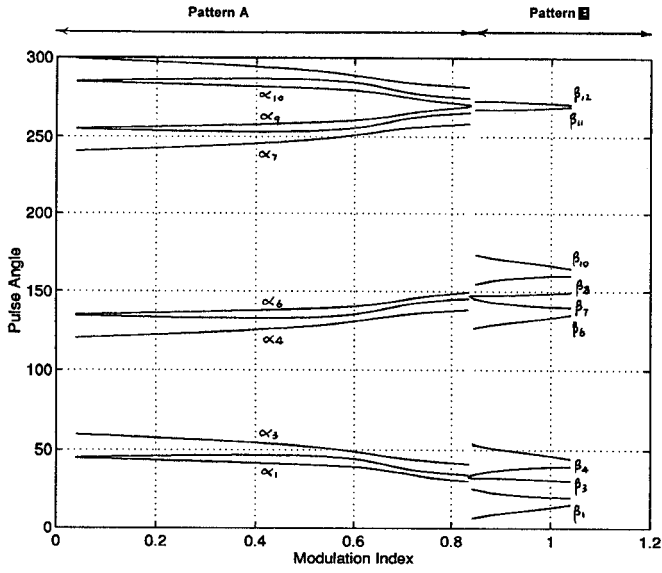
Fig. 4    Switching angles vs. modulation index

are no longer eliminated. Therefore, Pattern A and B can be combined to provide an adjustable dc current over a full range of modulation index, which is defined as

$$M_d = \frac{I_w}{I_d} \qquad (1)$$

where $I_w$ is the fundamental component of the converter input current and $I_d$ is the dc output current. Figure 5 shows the harmonic contents in the converter input current generated by Pattern A and B. Although these switching patterns can satisfy all the requirements, the 7th and 17th harmonic currents produced by Pattern B are relatively high, which may increase energy loss in the transformer secondary winding.

Figure 6 illustrates the harmonic content associated with Pattern A and C. Obviously, a better harmonic profile is achieved for Pattern B at the expense of increased switching frequency. Furthermore, the magnitude of harmonic currents changes with the modulation index smoothly, especially during the transit between the two patterns. Therefore, for the high power converters where a switching frequency of 420Hz can be implemented, the combination of Pattern A and C is recommended.

## IV. Resonant Modes and Capacitor Design

The filter capacitor and transformer inductances constitute the system resonant modes. Figure 7 shows the equivalent circuit for resonant mode analysis. The system admittance seen by the converter can be expressed as
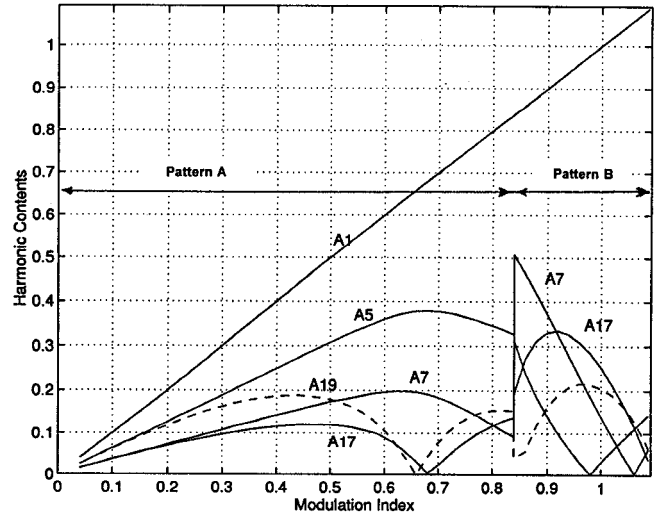


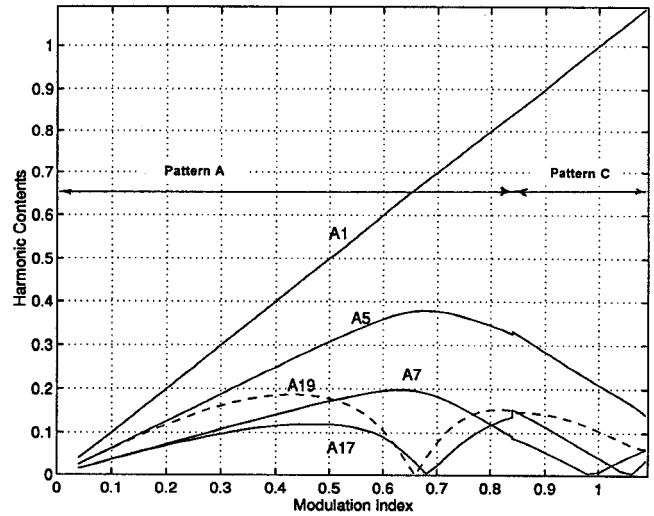Fig. 5    Harmonic contents of combined PWM Pattern A and B



Fig. 6    Harmonic contents of combined PWM Pattern A and C

$$Y(s) = SC + \cfrac{1}{SL_2 + \cfrac{1}{\cfrac{1}{SL_1} + \cfrac{SC}{S^2 L_2 C + 1}}} \qquad (2)$$

The zeros of the admittance $Y(s)$ represent the parallel resonant modes. The frequencies of these resonant modes can be calculated by

$$\omega_1 = \frac{1}{\sqrt{L_2 C}} \qquad (3)$$

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and

$$\omega_2 = \frac{1}{\sqrt{(2\,L_1+L_2)\,C}} \cdot \qquad (4)$$

The first resonant mode is associated with the transformer secondary leakage inductance only. This resonance may be excited by the harmonics in the converter input current $I_w$. Since the 11th and 13th harmonic currents in $I_w$ are eliminated, the frequency of this resonant mode may be set to

$$\omega_1 = 11 \sim 13 \; per \; unit.$$

Assuming the secondary leakage inductance $L_2$ is 0.05 per unit, the capacitor size can be determined by

$$C = \frac{1}{\omega_1^2\,L_2} = 0.12 \sim 0.17 \quad pu. \qquad (5)$$

This equation also indicates that the capacitor size could be reduced by increasing the transformer secondary leakage inductance, which can be achieved by transformer design. The transformer winding can be arranged in such a way that some of the primary leakage inductance can be moved to the secondary without increasing the cost of the transformer.

The second resonant mode is dominated by the total inductance $L_1$ on the transformer primary side including the inductance of the utility supply. Assuming $L_1 = 0.15$ per unit, the resonant frequency is

$$\omega_2 = \frac{1}{\sqrt{(2L_1+L_2)C}} = 4.1 \sim 4.9 \; pu \qquad (6)$$

Since the current in primary winding does not contain any harmonics lower than 23rd, this resonance will not be excited.

The resonant frequencies given in Equations (3) and (4) are derived under the assumption that the equivalent Y- and $\Delta$-connected secondary leakage inductances (refer to Fig. 7) have the same value. Generally, a transformer designer can easily make these inductances equal. However, in manufacturing, a few percentage of discrepancy may occur. In what follows, the effect of such a discrepancy on the resonant frequency is discussed. Assume that the Y- and $\Delta$-connected secondary leakage inductances can be expressed as

$$L_Y = L_2 \qquad (7)$$

and

$$L_\Delta = (\,1\,+\,K\,)\,L_2 \qquad (8)$$

where K represents the discrepancy in percent.

Following the same procedure discussed at the beginning of the section, the frequencies of the resonant modes can be calculated by

$$\omega_1 = \frac{1}{\sqrt{CL_2}} \cdot \frac{1}{\sqrt{1+\dfrac{L_1K}{2L_1+L_2(1+K)}}}$$

$$\approx \frac{1}{\sqrt{CL_2}} \cdot \frac{1}{\sqrt{1+K/2}} \qquad (9)$$

and

$$\omega_2 = \frac{1}{\sqrt{2C(L_1+L_2\dfrac{1+K}{2+K})}}$$

$$\approx \frac{1}{\sqrt{C(2L_1+L_2)}} \cdot \sqrt{\dfrac{1+K/2}{1+K}} \qquad (10)$$

If the secondary leakage inductances have a 5% discrepancy, $\omega_1$ and $\omega_2$ will change 1.2% approximately. Obviously, this change has little effect on the converter operation.
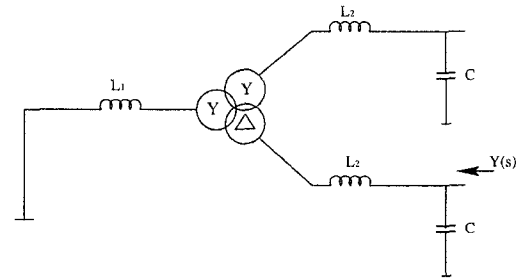


Fig. 7    Equivalent circuit for resonant mode analysis

## V. Input Power Factor Control

It is well known that a capacitor bank is required in current source converters to assist the commutation of switching devices. The use of the capacitor will make the input power factor leading. In the proposed converter system, a relatively small size capacitor can be used, even though the switching frequency is only 360Hz or 420Hz. This feature will facilitate the implementation of unity power factor operation. With a typical capacitor value of 0.15 per

unit for each converter, the converter system will have a leading input power factor of 0.96 under rated load conditions. To achieve unity power factor, a phase shift control can be integrated with modulation index control [7,8]. A small phase shift between the converter input voltage and modulated current will make the input power factor unity. The power factor control scheme proposed in [8] has been implemented in the dual converter topology.

## VI. Simulation and Experimental Results

Figure 8 shows a set of the simulation results. The converter system is rated at 4160V (line-to-line), 60Hz, and 1000kVA. The parameters used in the simulation are: $L_1 = 0.15$, $L_2 = 0.05$, and $C = 0.13$, all in per unit. Switching Pattern B is selected with the modulation index set at 0.9, at which both 7th and 17th harmonics have a large magnitude (the worst operating condition). The waveforms of converter input current $I_{wy}$, transformer secondary current $I_{sy}$ and secondary line-to-line voltage $V_y$ are shown in Figure 8(a) to (c), respectively. Although the secondary current $I_{sy}$ contains harmonics, these harmonics can be cancelled by the Δ-Y connected transformer. Therefore, the line current $I_s$ on the primary side is sinusoidal. The unit power factor is obtained by introducing a small delay angle between the converter input current and voltage.

The experimental results are obtained from a laboratory GTO dual current source converter system. The control of the laboratory system, including PWM gate pulse generator, PI controllers and a unity power factor controller, is implemented by a TMS320C31 based DSP board. All three switching patterns proposed in this paper are included in the PWM generator. The converter system is rated at 208V, 20kVA and 60Hz with $L_1 = 0.026$, $L_2 = 0.051$ and $C = 0.15$ per unit. The waveforms of converter input current $I_{wy}$, transformer secondary current $I_{sy}$, and line input current $I_s$ when the system is operated at $M_d = 0.857$ with Switching Pattern A are shown in Fig. 9. It can be seen that the line input current is nearly sinusoidal.

To investigate possible resonances which may be caused by the resonant modes during transient, a step command is applied to the converter system. Figure 10 shows one set of such experiments. The dc current $I_d$ is increased from zero to 32A in 40ms. The transformer primary line current $I_s$, secondary line current $I_{sd}$ and converter input current $I_{wd}$ do not exhibit any resonant phenomenon during transient. Many experiments were performed under various loading conditions with a step increase or step decrease command. No resonant phenomenon were ever observed during the experiments.
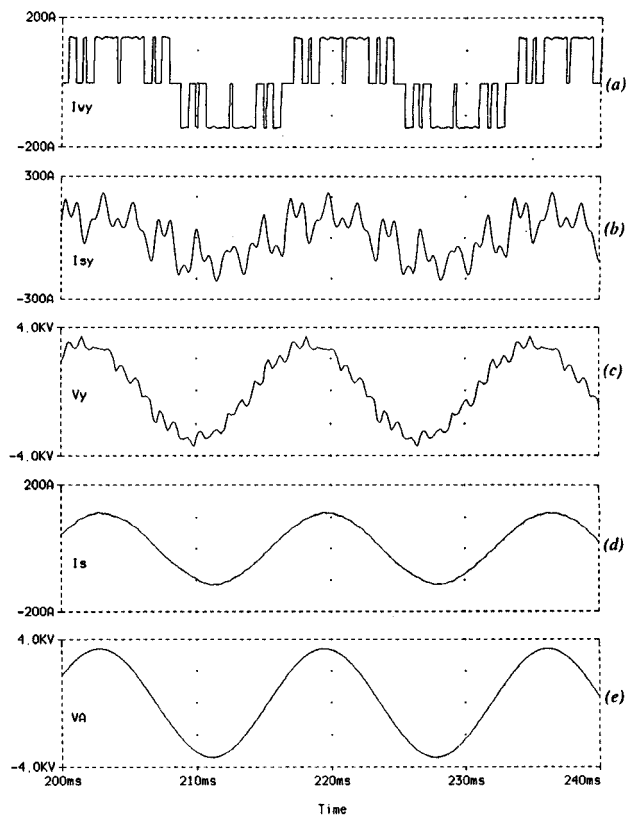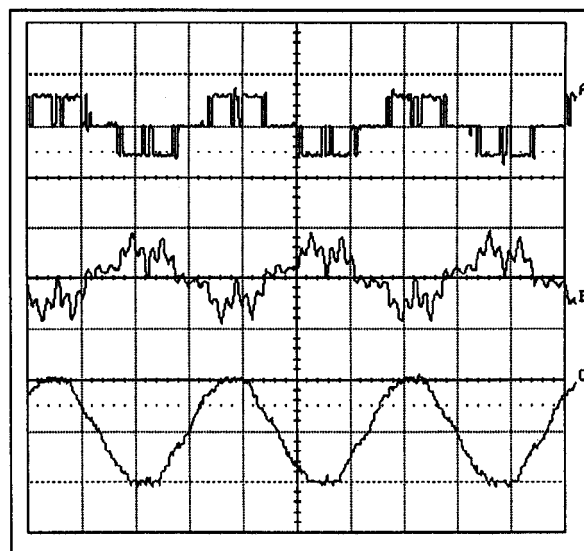


Fig. 8  Simulation results from a 4160V, 1MVA converter system: Pattern B at $M_d = 0.9$ ( the worst operation condition)



Trace:  A:Converter input current $I_{wy}$      50A/div  5ms/div
B:Transformer secondary current $I_{sy}$  50A/div  5ms/div
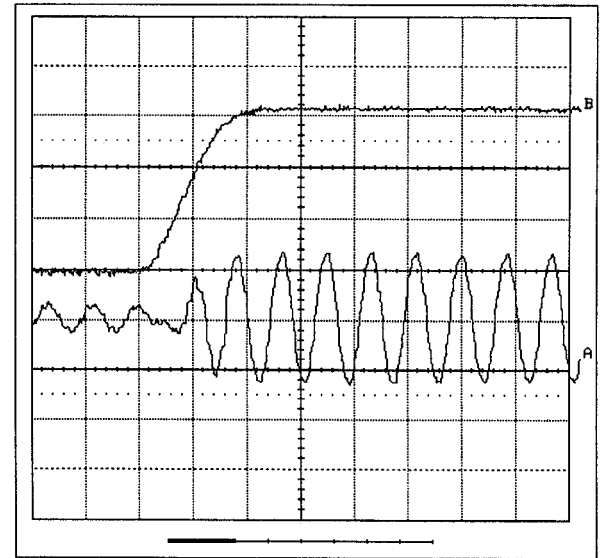C:Line current $I_s$                 50A/div  5ms/div

Fig. 9  Experimental results from a 208V, 20kVA dual converter system: Pattern A at $M_d = 0.857$

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## VII. Conclusions

A dual GTO current source converter topology with sinusoidal inputs is proposed for high power applications. The sinusoidal input current is realized by using PWM techniques to eliminate 11th and 13th harmonics and a transformer to cancel 5th, 7th, 17th and 19th harmonics. Three switching patterns are proposed with switching frequency of 360Hz and 420Hz. The combination of these switching patterns provides a full range control over the dc output current. Resonant modes of the proposed system are identified and the criterion for the line capacitor design is provided. A unity power factor control scheme for the proposed topology is briefly discussed. A DSP-based 20kVA dual current source converter system has been constructed to verify the theoretical analysis. The proposed topology is particular suitable for high power applications due to its low switching frequency, sinusoidal inputs and easy unity power factor control.

## References:

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(a)

Trace:    A: Line current $I_s$    50A/div  20ms/div
          B: DC current $I_d$     10A/div  20ms/div
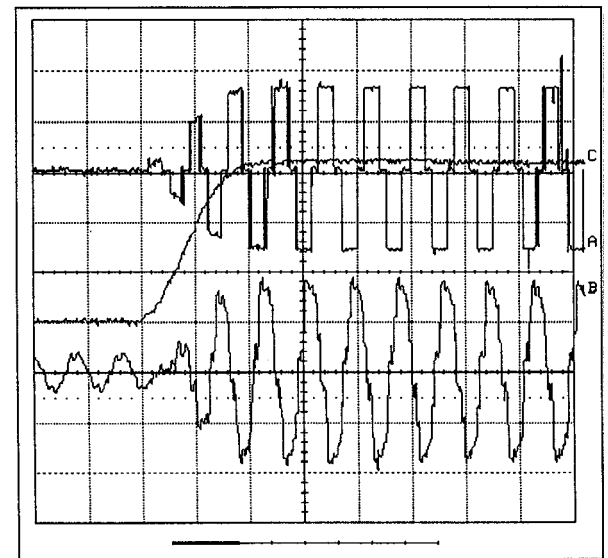


(b)

Trace:    A: Converter input current $I_{wd}$    50A/div  20ms/div
          B: Transformer secondary current $I_{sd}$  50A/div  20ms/div
          C: DC current $I_d$                      50A/div  20ms/div

Fig. 10    Step response of laboratory dual converter system for the investigation of resonant modes, Pattern B at $M_d = 1.075$