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GLOSSARY

ADC	Analogue to digital converter
BER	Bit error rate
BJT	Bipolar junction transistor
CMOS	Complementary metal-oxide semiconductor
CM	Current-mode
CMFB	Common mode feedback
CMFF	Common mode feed through
CMRR	Common mode rejection ratio
CT	Continuous-time
DO	Dual output
DSP	Digital signal processing
EPR4	Extended partial response 4
E^2PR4	Extended-extended partial response
FBDDA	Fully balanced differential difference amplifier
FLF	Follow the leader feedback
FOM	Figure of merit
FIR	Finite impulse response
GDR	Group delay ripple
GSM	Global system for mobile communications
GFSK	Gaussian frequency shift keying
GMSK	Gaussian minimum shift keying
HDD	Hard disk drive
HF	High frequency
ISI	Inter-symbol interference
IFLF	Inverse follow the leader feedback
LV	Low voltage
LP	Low power
LF	Leap frog
LNA	Low noise amplifier
MLF	Multiple loop feedback
MIMO	Multiple input multiple output
MO	Multiple output
NSDR	Negative source degeneration resistor
NMOS	N type complementary metal-oxide semiconductor
OFDM	Orthogonal frequency division multiplexing
Op-amp	Operational amplifier
OTA	Operational transconductance amplifier
PRML	Partial response maximum likelihood
PMOS	P type complementary metal-oxide semiconductor
PR4	Partial response 4

PSRR	Power supply rejection ratio
PS	Power supply
PC	Power consumption
RF	Radio frequency
SC	Switched capacitor
SNR	Signal to noise ratio
SoC	System on chip
SISO	Single input signal output
UHF	Ultra high frequency
UWB	Ultra wideband
VCCS	Voltage control current source
VHF	Very high frequency
VGA	Variable gain amplifier
WCDMA	Wideband code division multiple access
WLAN	Wireless local area network

1. Introduction

1.1 Background

Filters are used in any electronic system where it is necessary to control the bandwidth of the signal path. Filters are frequency-selective electronic circuits designed to pass a band of wanted signals and stop or reject unwanted signals, noise or interference outside the passband [1-25]. Filters appeared at the earliest stages of the development of electronics, and have played an essential role in many fields. In recent years, the rapid advances in computer hard disk drive (HDD) [26-63] and wireless communication systems [64-103] in particular have resulted in considerable demand for higher performance filtering circuits.

In general, filters are classified according to the function they perform. Over the frequency range of interest of a filter, we define passband and stopband. Ideally, the passband of a filter is the range of frequencies over which signals are transmitted from input to output without attenuation or gain. Note that in practice, active devices may be used to achieve gain or amplification. In the stopband, the transmitted signal is highly attenuated. The disposition of passbands and stopbands lead to the four most common types of filter classification. These are lowpass, highpass, bandpass, and bandstop (or also referred to as notch) filters. There are other kinds of filters, but their filtering actions are based on and can be described in terms of the four most basic types.

Active-RC filters have been widely used in low-frequency applications for a long time [63, 76-86]. Discrete active-RC filters were successful substitutes for passive-RLC filters at low audio frequencies for reasons of size and economy. However, they were found less suitable for high-frequency applications and fully integrated implementations due to the high frequency limitations of op-amps and the large chip area requirements of resistors. Consequently, many alternative active filter circuit topologies have been developed to overcome these drawbacks, for example the

popular switched-capacitor filter. In switched-capacitor filter structures, MOS switches and capacitors effectively replace the resistors (unsuitable for full integration) in active-RC filter structures. Nowadays, switched-capacitor filters can be fully integrated using all available IC technologies especially CMOS. In addition, precision frequency response is achievable without on-chip tuning, and high dynamic range can be achieved. However, they are still not suitable for very high frequency applications due to the sampling mode of their operation, which would require very high clock speeds, along with the use of extra continuous-time (CT) input anti-aliasing filters and output smoothing filters.

CT filters based on the operational transconductance amplifier (OTA) (also referred to as V-I converter, transconductor, or transconductance amplifier) and capacitors, the so-called OTA-C, or gm-C, filters have received the greatest interest and attention in recent research [1-4, 31-110]. OTA-C filters offer advantages over traditional active-RC filters in terms of design simplicity, high frequency capability, electronic tunability, suitability for monolithic integration, reduced component count, and potential for design automation. Although OTA-C filters are primarily aimed at high frequency operation (up to GHz range), they are also suitable for applications at low frequencies. One of the most important recent applications of fully integrated OTA-C filters is as equalizers in HDD read channels. Also, fully integrated OTA-C filters have been widely used in communication systems [87-103].

The performance of a filter relies strongly on the circuit components, filter structure, design methods, and IC technology used. In particular, different circuit components and IC technology can result in very different performances for the chosen filter topology. The design of a high performance OTA-C filter is a complex task. It must simultaneously optimize different requirements, such as operating frequency range, power consumption, noise and dynamic range, sensitivity to device variations and fabrication tolerances, chip area, and cost. A number of IC technologies such as Bipolar [26, 27], BiCMOS [28-32, 94], CMOS [33-63, 65-69, 77-85, 87-93, 95-103],

GaAs, etc have been used for integrated filter design. Currently, there is great emphasis on implementing integrated filters using sub-micron digital CMOS technologies, even though these are not optimized for analogue applications. This is because analogue filters are usually components of complex mixed-signal "systems on chips", where the majority of the chip area contains digital circuits. Therefore there is an overwhelming case to use an IC technology that is low cost and compatible with high density digital logic, to achieve economy and maximum integration. CMOS provides favorable characteristics for high density integration such as low power supply voltage and low static power dissipation for digital circuits [6]. However, CMOS devices have a low driving current, which is a drawback for high speed applications.

Other technologies offer potential advantages for high speed analogue design. GaAs technologies offer very high speed. However, complementary N- and P-channel enhancement mode devices are not are not possible in current GaAs technologies, leading to logic circuit structures that require level-shifting and DC bias currents under static operating conditions. Therefore GaAs gates are more complicated than CMOS, and consume significant power under static conditions, making GaAs unsuitable for high density, low power mixed signal designs [135]. Bipolar technologies offer the advantages for high frequency operation of higher transconductance and current drive for a given device size and bias current. The main limitations of Bipolar technologies include low integration density, high cost, and high power. BiCMOS combines some of the advantages of bipolar and CMOS technologies. However BiCMOS processes are less well developed than pure CMOS, leading to lower integration density and higher cost. Therefore, CMOS has now become the preferred technology for analogue design. Practical analogue filters are typically designed in CMOS technologies requiring supply voltages at or below 3.3V. Most analogue or mixed-signal systems are power critical, and power consumption is limited to a few milliwatts. The frequency capability of integrated analogue active filters (depending on the design and the type of active and passive devices used) can

span from low audio frequencies to the GHz range. Note that the frequency limits of active filters tend to improve as technology advances and faster active devices become available. In terms of sensitivity to component variations and fabrication tolerances, passive-RLC filters feature the lowest degree of sensitivity. However, they are not compatible with currently available integrated electronics. In most practical CT filters, an on-chip automatic tuning system is incorporated to overcome performance degradation due to device variations and fabrication tolerances as well as the effects of parasitics, temperature, and environment changes. Moreover, using the right filter structures can also reduce sensitivity. Low supply voltages have adverse consequences for active filter design. As the supply voltage shrinks, the linear signal range of the active devices also decreases. Consequently, the available dynamic range (defined as the ratio of maximum over minimum signal level) is reduced. The minimum signal is restricted by noise, which is generated by active devices and resistors, and does not show a corresponding reduction at lower supply voltages.

1.2 Developments in High Frequency OTA-C Filters

Motivated by the rapidly growing HDD, mobile and wireless communication market, fully integrated filters for very high frequency (at the time of writing up to 800MHz) and low power consumption applications have received considerable worldwide attention. Increasing HDD data rates and density, and radio spectrum occupancy requires that other aspects of filter performance be improved, such as dynamic range and resistance to intermodulation. Design techniques must also utilize current IC technologies. The move to deep sub-micron CMOS technologies increases the speed capability of analogue circuits, but also introduces new problems. For example the reduction in supply voltages will lead to reduced signal voltage swing and dynamic range, and reduced DC gain due to short channel effects.

The most important filters for fully integrated high frequency applications are perhaps the OTA-C filters, which have been extensively investigated and widely utilized. Structure generation, design methods, performance analysis and comparison

of OTA-C filters have been extensively investigated. Many second-order (biquad) OTA-C filter circuits have been developed. Structure generation and design of high-order OTA-C filters based on the cascades of biquads, LC ladder simulation, and multiple loop feedback (MLF) methods have been explored. Practical design considerations for high-frequency OTA-C filter structure generation lead to use of grounded capacitors and minimum component count. Note that grounded capacitors require smaller chip area than their floating counterparts. In addition, all high impedance internal nodes of the filter structure have a grounded capacitor, within which parasitic capacitances at that node can be absorbed. Minimum component or canonical filter structures have the advantages of reduced power consumption, chip area, noise and parasitic effects compared to their non-canonical counterparts. Other considerations require the design method and equations should be simple. Note that non-canonical filter architectures are required in some applications to achieve some design flexibilities or to meet special specifications. Most of the current research is concerned with realization of high-order OTA-C filters.

OTA-C filters also have significant limitations. Good overall linearity of the transfer function of OTA-C filters is only achievable with highly linearized OTAs. Increased linear range will unavoidably decrease the available range of transconductances of the OTAs at a given supply voltage, and increase OTA noise**.** As with other types of active filter, errors in the desired filter response may occur at high frequency, due to excess phase caused by device and layout parasitics at high frequencies. In common with other integrated filters, errors in filter response may be caused by device tolerances, process, temperature and bias effects. Overcoming this problem requires the use of on-chip tuning circuits in most applications. Fully-differential OTA-C filter structures are normally used to reduce noise from on-chip digital circuitry and power supply. Many OTAs with improved linearity for dynamic range enhancement of OTA-C filters have been reported. Despite such advances, the stringent requirements (LV/LP, VHF, higher DR, etc) pose challenging task for OTA-C filter designers. In an OTA-C filter, the transconductance values of

OTA cells determine the pole frequencies of the filter together with the capacitor values. Unfortunately, the available range of transconductances becomes small as the supply voltage is reduced, and the parasitic capacitances become a large proportion of the total nodal capacitance at high frequencies. Thus, OTA-C filters are expected to be limited in VHF and UHF range with pure CMOS technology.

In recent years, current-mode signal processing has received considerable interest due to the superior performance (bandwidth and dynamic range), LV/LP operation, and simple circuit structure, compared to its voltage-mode counterpart. Dual-output OTAs (DO-OTAs) [105] and multiple-output OTAs (MO-OTAs) [106, 107] have been utilized to generate current-mode CT filters [43, 55-60, 104-108]. Early work was mainly concerned with current-mode DO-OTA-RC filters, whilst more recent work involves current-mode biquadratic and MLF filters using DO-OTAs and biquadratic, MLF and ladder filters using MO-OTAs. These current-mode DO-OTA-C and MO-OTA-C filters, which have the benefits of both the normal OTA-C technique and the current-mode approach, have good potential for future high frequency integrated filtering applications.

1.3 Research Scope

OTA-C filters designed using the biquad cascade method have high sensitivity whilst those using the LC ladder simulation method cost more power consumption and chip area due to the need for extra OTAs to convert floating capacitors to grounded ones [1]. It has been shown that the MLF OTA-C filters have low sensitivity and are able to implement arbitrary zeros. Note that non-imaginary-axis zeros are required, for example, in equaliser design for HDD read channels. Thus, the research in this thesis is focused on the design and performance of high-order high-frequency CMOS MLF OTA-C filters. Specifically, design and applications of current-mode leap-frog (LF), current-mode follow-the-leader-feedback (FLF), voltage-mode inverse-follow-the-leader-feedback (IFLF) and voltage-mode LF MLF

filter structures are studied. Filter design and simulations of tunable linear CMOS OTAs are also presented.

In the area of current-mode MLF filter design, LF and FLF filters are considered. Synthesis and design of the general all-pole and arbitrary zeros current-mode LF OTA-C filters are particularly studied. In order to implement these OTA-C filters, three tunable CMOS OTA designs featuring high frequency responses are presented and their simulation results are obtained. Multiple differential output and multiple differential input OTAs were developed for design of fully-differential current- and voltage-mode filters respectively. Performance analysis in terms of transconductance range, noise, dynamic range, etc of the OTAs are also given. As examples, several specific OTA-C filters realizing different filtering characteristics are designed and simulated, among which are fifth- and seventh-order 0.05° equiripple linear phase LF, FLF and IFLF equalizers with programmable gain boost for computer HDD read channel applications, and fifth-order elliptic FLF and IFLF lowpass filters for wireless communication receiver baseband applications.

1.4 Original Contributions

The research has led to several novel contributions.

- Designs of a 400MHz seventh-order voltage-mode IFLF and a 150MHz seventh-order current-mode FLF 0.05° equiripple linear phase filters with novel fully-differential OTAs for computer HDD read channels are proposed.
- The general design formulas for current-mode MLF LF structures and explicit design formulas for up to the sixth-order of them are derived.
- Two 750MHz fifth-order current- and voltage-mode MLF LF 0.05° equiripple linear phase lowpass filters for computer HDD read channels are proposed.
- Two fifth-order current-mode FLF, LF and voltage-mode IFLF, LF elliptic filters for wireless communication baseband are designed.

The following is a listing of all publications that have resulted from this work:

- Y. Sun and X. Zhu, “Explicit design formulas for current-mode Leap-frog Gm-C filters and 300MHz CMOS seventh-order linear phase filter,” Int. J. Circuit Theory and Applications, accepted.
- X. Zhu, Y. Sun, and J. Moritz, “ A CMOS Fifth-order 750MHz Current–Mode LF Filter for Hard Disk Read Channels,” Proc. IEEE ISCAS, Seattle, May 2008.
- X. Zhu, Y. Sun, and J. Moritz, “ A 0.18μm CMOS 300MHz Current–Mode LF Seventh–order Linear Phase Filter for Hard Disk Read Channels,” Proc. IEEE ISCAS, New Orleans, May 2007.
- X. Zhu, Y. Sun, and J. Moritz, “A CMOS Fifth-Order 400MHz Current-Mode LF Linear Phase Filter for Hard Disk Read Channels,” Proc. IEEE ECCTD, Seville, August 2007.
- X. Zhu, Y. Sun, and J. Moritz, “A CMOS 650 MHz Seventh-order Current-Mode 0.05° Equiripple Linear Phase Filter,” Proc. MWSCAS, Montreal, August 2007.
- X. Zhu, Y. Sun, and J. Moritz, “A 0.18μm CMOS 9mW Current Mode FLF linear phase filter with gain boost” Proc. MWSCAS, Montreal, August 2007.

1.5 Organization of this Thesis

This thesis consists of eight chapters. They are organized as follows:

Chapter 1, this chapter, gives the background and scope of the research.

Chapter 2 reviews analogue filters for computer HDD read channel, including design considerations and a summary of the state of the art of OTA-C read channel filters.

Chapter 3 presents synthesis, design, and performance of current-mode FLF and voltage-mode IFLF OTA-C filters using a novel fully-differential OTA.

Chapter 4 includes the derivation of design formulas for current-mode all-pole and arbitrary transmission zero LF OTA-C filter structures, with a detailed design example of a seventh-order 0.05° equiripple linear phase lowpass filter for computer HDD read channels. The design and simulation of a tunable fully-differential CMOS OTA are also given.

Chapter 5 describes two UHF fifth-order 0.05° equiripple linear phase LF lowpass

OTA-C filters, in current- and voltage-mode respectively, for next generation computer HDD read channel applications.

Chapter 6 reviews analogue filter design for wireless communication receivers; multi-standard analogue baseband channel select filters are particularly investigated. The summary of previous works and comparison of active-RC and OTA-C filters for this application are also discussed.

Chapter 7 describes four fifth-order elliptic OTA-C filters based on current-mode FLF, LF and voltage-mode IFLF, LF configurations, which are intended for use in the receiver baseband section of advanced integrated wireless transceivers.

Chapter 8 contains conclusions to the thesis and suggests some further research topics.

2. Review of Analogue Filters for Computer Hard Disk Drive Systems

2.1 Introduction

Storage devices have been divided on the basis of their performance, typically specified in terms of the access time to the stored data, and cost quoted in terms of $/Mbyte. Figure 2.1 shows the division of some commonly used storage devices. Cost sensitive application such as data distribution and entertainment music use devices such as the CD-ROM, which have high access time and are low priced. Tape storage and backup systems use lower performing systems; however, hard disk drive (HDD) systems are high performance systems and support near real-time applications [45]. HDD systems continue to develop at a rapid and deterministic pace to meet the emerging demands of high performance computing and peripheral devices.

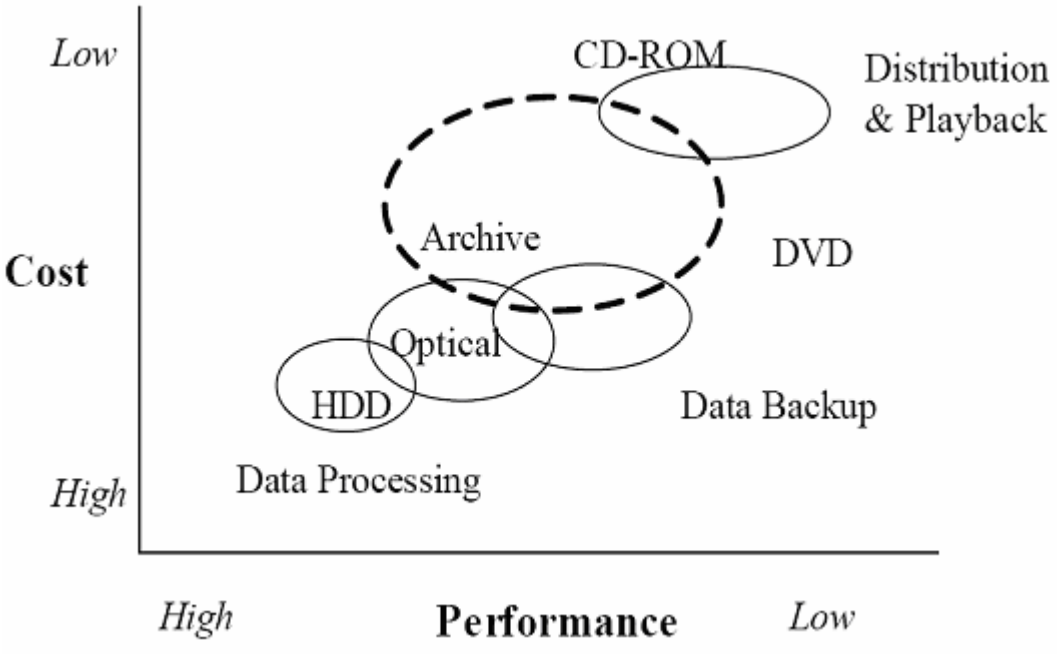


Figure 2.1 Storage system segmentation [45]

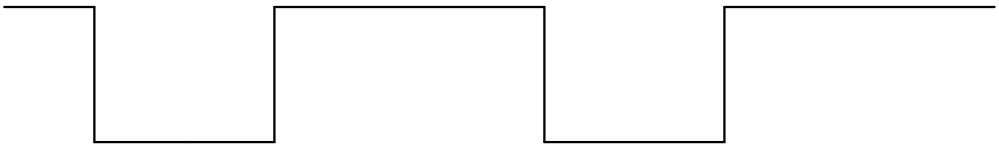
In this chapter, design considerations for very high frequency filters for next generation HDD read channels are addressed. The chapter is organized in the

following way: Section 2.2 addresses the architecture of HDD read channels. Some previous work on analogue filters for computer HDD systems is summarized in Section 2.3. In Section 2.4, filter design considerations for read channel OTA-C filters such as group delay responses, transfer function of the filter, filter architectures, filter circuits and tuning are discussed. OTA design considerations for read channel OTA-C filters are also discussed in Section 2.5. Finally, the chapter is concluded in Section 2.6.

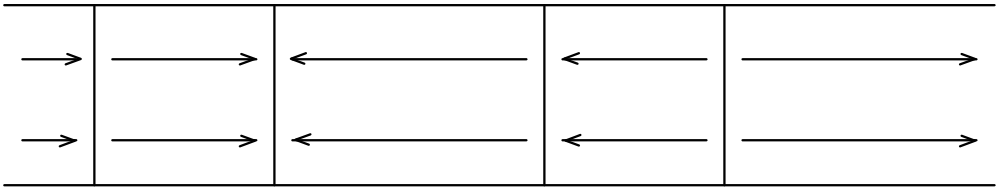
2.2 Architecture of Hard Disk Drives

The read channel chip is a very important part of a HDD system. Advances in read channel technology have lead to increases in density of the HDD by more than 50% over the last few years. Read channel design is evolving at a very fast pace to keep up with other advances in HDD technology. The peak detection method in read channel enjoyed widespread use for more than 30 years. It was replaced by partial response maximum likelihood (PRML) method, which was subsequently replaced by the more powerful extended PRML. In computer data storage, PRML is a method for converting the weak analogue signal from the head of a magnetic disk or tape drive into a digital signal. PRML attempts to correctly interpret even small changes in the analogue signal, whereas peak detection relies on fixed thresholds. Because PRML can correctly decode a weaker signal it allows higher density recording [132]. The current trend is based on combining channel coding and equalization. The magnetic media and preamplifier stage of the HDD system can be considered as a bandwidth-limited channel. Data is recorded on the magnetic media using binary amplitude levels. The read back signal is analogue. This signal is corrupted by distortion, noise and interference. The read channel involves extensive signal processing to assist extraction of reliable binary data from the magnetic media. The corrupting noise in the signal includes electronic noise and media noise, but the biggest source of signal corruption is inter-symbol interference (ISI). The magnetic material on a hard disk is divided in concentric, circular tracks. These tracks are

magnetically saturated in one of two directions: clockwise or counter clockwise along the track. Because the magnetic medium is always saturated, its magnetic hysteresis can be ignored. This approach is called saturation recording and shown in Figure 2.2 [133].



(a) Two level write current



(b) Magnetisation on track

Figure 2.2 Saturation recording (a) Two level write current (b) Magnetization on track

The data is represented differentially: 1-bits are indicated by a change in magnetization, for 0-bits the magnetization is left untouched. This representation is referred to as non-return to zero write current (NRZI) modulation. The consequence is that when the disk is spinning under the read head, a 1-bit gives rise to a pulse, a 0-bit does not. The most straightforward scheme of data reconstruction is therefore peak position detection [48].

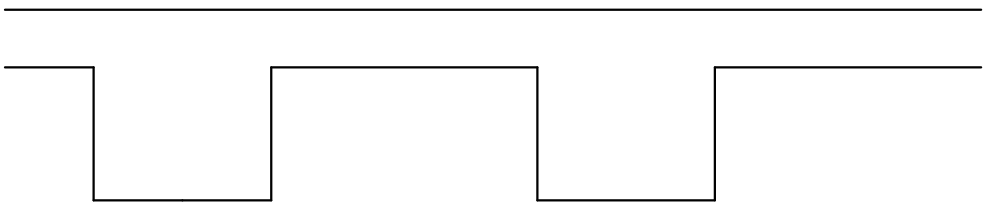


Figure 2.3 NRZI recording

However, as the bit density of the hard disk increases, the time between two pulses

becomes smaller. In that case, the overlap of the pulses increases. This is called inter-symbol interference (ISI). Figure 2.4 shows ISI diagrammatically. An eye diagram, which overlays many samples of a signal can give a graphical representation of the signal characteristics. In Figure 2.5, eye diagrams with and without ISI are shown.

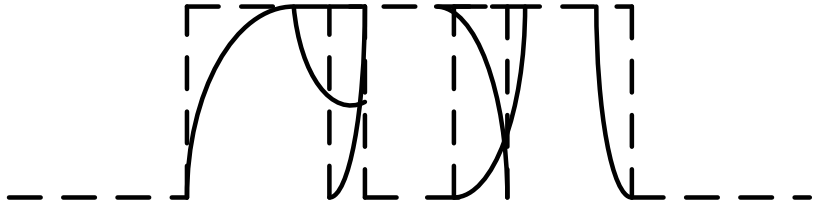
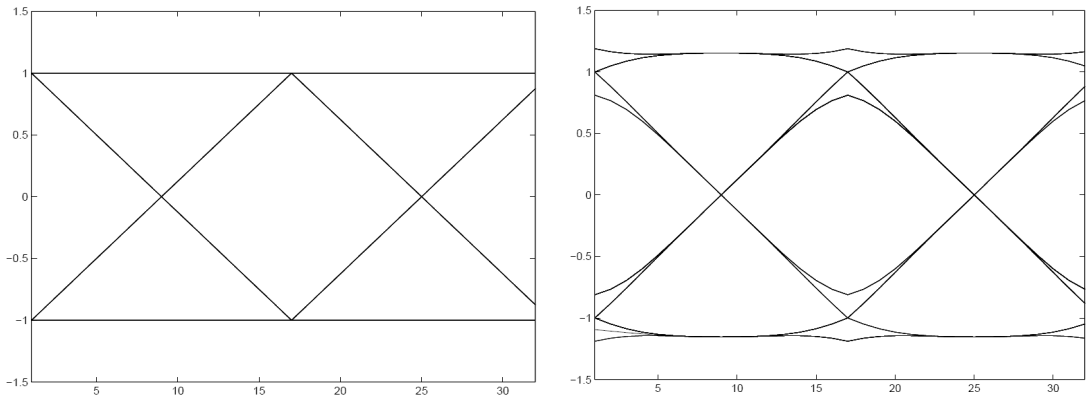


Figure 2.4 Diagram of inter symbol interference (ISI)



(a) (b)

Figure 2.5 (a) Eye diagram without ISI, (b) Eye diagram with ISI

At higher linear densities, the linear model of the magnetic recording channel breaks down. Since the binary signal transitions are at closer spacings due to ever increasing data density, the read back signal amplitude contains greater ISI. This degrades the signal to noise ratio (SNR), resulting in a higher bit error rate (BER). BER is the ratio of the number of bits incorrectly received to the total number of bits received during a specified time interval. Signal processing can only marginally compensate for the effect of ISI. Hence ISI is by far the dominant source of errors in high-density recording. The PRML technique, which helps in reducing ISI, is used widely in

industry [38-42, 47-52, 54-59]. Most schemes use an analogue to digital converter (ADC), a finite impulse response (FIR) filter and a continuous-time (CT) filter for channel equalization. Most of the equalizer architectures use a CT OTA-C filter, because of their higher frequency and simplicity, modularity and easy programming of the biquads involved.

In this thesis we will present the design of a high frequency 0.05° equiripple linear phase OTA-C based lowpass filter used for equalization in HDD systems. As mentioned earlier PRML technique allows us to increase the data density by up to 100% as compared to peak detect methods. However, achieving this increase requires better channel equalization and detection techniques. A large number of such techniques have been reported in the literature utilizing primarily analogue or analogue and digital methods. Some of them employ multiple chip [31] [34] or discreet external block [29] solutions. A predominantly analogue design can help in reducing the cost and also avoid the noise-related issues involved with mixed mode design. One of the commonly used PRML based mixed-mode read channel paths [40] is shown in Figure 2.6.

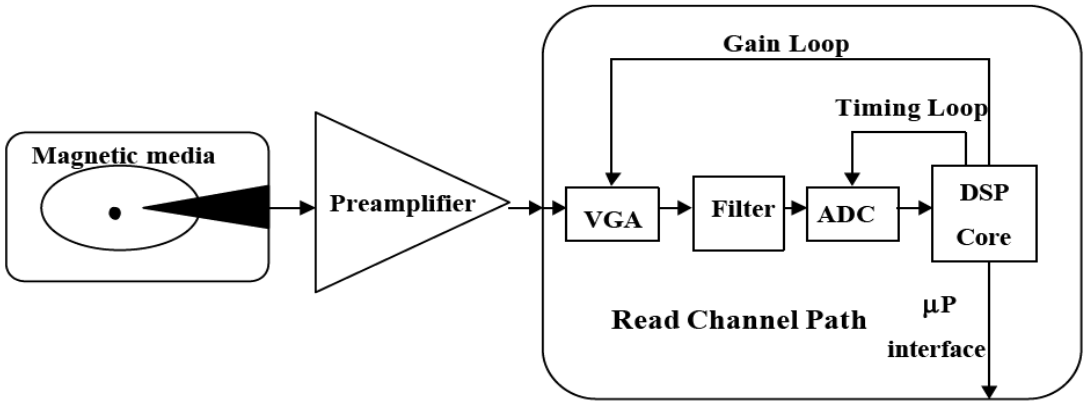


Figure 2.6 Architecture of HDD analogue front-end

The above figure shows the analogue front-end pulse processing with digital data detection. The preamplifier block along with noise reduction amplifies the signal from the magnetic media read head. This signal is then fed into the variable gain amplifier

(VGA). The amplified signal is then applied to a low pass filter. One role of the filter is to minimize the incoming noise from the media, preamplifier, and VGA, effectively increasing the SNR of the signal and therefore reducing the BER. A second role of the filter is to perform signal equalization, which partly compensates for the bandwidth limitations of the media and preceding amplifiers, in order to slim the data pulses, allowing higher bit densities. The signal then undergoes A/D conversion, typically with 6-bit resolution. The digital signal processor (DSP) core can perform additional equalization in the digital domain, if necessary, and implements the data detector. It also controls gain and timing as well as communication with the interface. The equalization task involves trade-offs between the design of the analogue filter and the digital FIR filter. The analogue filter can be made more complex to improve the performance and this will relax the requirement on the power consumption, complexity and order of the digital FIR filter for a given silicon area. In certain applications, the analogue filter performs only the task of a noise anti-aliasing filter while the equalization task is done completely in the digital domain. However, if a significant amount of equalization is done in the digital domain then the quantization noise produced by the ADC is enhanced by the digital FIR filter. This results in increased complexity and resolution of the ADC to reduce the quantization noise contribution. The cut-off frequency of the filter should be tunable over a wide range in order to take full advantage of read channels utilizing constant density recording techniques. Since the disk rotates at a constant speed, data recorded in the outer tracks, where the disk is moving at higher speed relative to the read head, is read at a higher rate than data close to the center of the disk. Therefore, the lowpass filter plays a very important role in the analogue domain and researchers have made much effort to achieve improved performance, particularly to increase the system bandwidth. Therefore, the overall performance of the computer HDD read channel depends on the individual system blocks. The minimum requirements of each block in Figure 2.6 are summarized in Table 2.1.

Table 2.1 Summarized minimum requirements for each block in Figure 2.6

Block	Minimum requirements
VGA	40dB gain with a nominal level of $1V_{p-p}$
Filter	4^{th} to 8^{th}-order with 35dB dynamic range and 2:1 tuning range
ADC	5 or 6 bit resolution, 16 to 22dB SNR
DSP core	3 to 10 tap FIR filter

Presently in most designs, equalization is done mostly in analogue domain, as it is currently easier to implement high frequency analogue equalizer designs to perform the equalization task. The analogue filter is used to perform some or all of the equalization required to match the pulse shape data retrieved from the magnetic media to a target pulse shape. The usual target pulse shapes are Partial Response 4 (PR4), Enhanced Extended Partial Response 4 (EPR4) or Enhanced Extended Partial Response 4 (E^2PR4). Different partial response schemes are often described using polynomials. These polynomials historically came from digital signal processing. For example, for an input data pattern described in NRZ terms, "0" stands for one particular direction of medium magnetization and "1" for another. The data pattern is given by the sequence of bits a_k. When a magnetic head reads the signal, it responds only to the changes of magnetization, i.e. it differentiates the signal. The differentiating function of the head can be described if a "delay operator" D is introduced, given by $Da_k = a_{k-1}$. The head acts on the NRZ pattern as $(1-D)a_k = a_k - a_{k-1}$. This $(1-D)$ operation will result in +1 or -1 output samples, depending on the direction of the magnetization change. The $(1-D)$ operator is the simplest polynomial, corresponding to generating positive or negative samples. In a PR4 system each pulse of voltage has 2 samples. In other words, if a transition of magnetization occurs, it results in a sample equal to "1" at the transition location and another sample at the next sample period. This is equivalent to "spreading" or delaying and adding the

current sample, given by operator *(1+D)*. Indeed, if a_k =1, the operator *(1+D)* a_k will result in sequence "1,1". Therefore, a PR4 system in polynomial terms is described as $(1-D)(1+D) = 1- D^2$, where operator D^2 is the result of a product D times D and delays the current sample two bit periods: $D^2 a_k = a_{k-2}$. If we discard the differentiating part of the polynomial given by *(1-D)* and look only at *(1+D)* we will get the samples of the isolated pulse: {1, 1}. In other words, the term *(1+D)* determines how the transition samples are "spread" over the bit periods. PR4 is a particular case of more general family of PR polynomials, given by the general equation: $(1-D)(1+D)^n$. PR4 corresponds to n=1. If we set n=2 the samples of the isolated pulse will be given by the term $(1+D)^2 = 1+2D+D^2$, which corresponds to (1,2,1). This type of PRML is called EPR4. When n=3, the polynomial is given by $(1+D)^3 = 1+3D+3D^2+D^3$ and the isolated pulse has samples {1,3,3,1}. This type of partial response is called E^2PR4. Figure 2.7 shows the shape of an isolated pulse and then of two adjacent pulses [38, 48, 133]. Table 2.2 summarizes different PRML schemes used in magnetic recording.

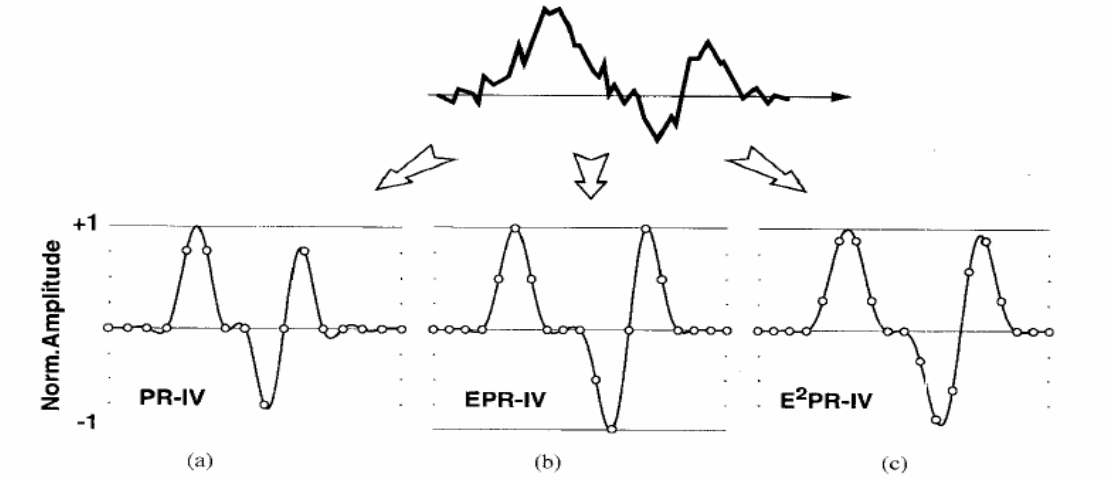


Figure 2.7 Common partial-response targets used in magnetic recording [48]

Table 2.2 Summarized different PRML schemes [133]

Name	Polynomial	Isolated Pulse Samples
PR4	(1-D)(1+D)	0 1 1 0…
EPR4	$(1-D)(1+D)^2$	0 1 2 1 0…
E^2PR4	$(1-D)(1+D)^3$	0 1 3 3 1 0 …

Approximate pulse symmetry is usually found in incoming pulses from the magnetic media. Consequently, the group delay of the filter is required to exhibit a relatively flat characteristic in the band of interest. Note that, for the case of HDD design, the read channel filters should have linear phase response to equalize data pulses and minimize pulse peak shift in time. The amount of amplitude equalization provided by the filter and the filter group delay must be independent of each other. The importance of this specification is motivated by the fact that the information content of the signal at the read head of a hard disk is held in the time at which pulses occur. If the group delay is not constant in the frequency band where the spectral components of the signal are located, the pulse might shift in time due to the equalizer. This means that the equalizer is affecting the information content of the signal. This is obviously unacceptable.

The lowpass filter response is extended with a boost function. This consists of selective additional gain for the frequencies around the cut-off frequency of the equalizer. The amount of gain boost is defined as the additional gain at the cut-off frequency relative to the low frequency gain. Boosting is done to shape the spectrum of the received signal according to the desired class of equalization of a read channel. In the time domain, the isolated read pulse can be slimmed and made symmetrical. This is equivalent to high-frequency boost in the frequency domain [134]. The diagram of the lowpass filter with and without gain boost is shown in Figure 2.8. It consists of a selective additional gain for the frequencies around the cut-off frequency of the filter. The amount of boost is defined as the extra gain relative to the low frequency gain at the cut-off frequency. The boost function should not affect the ripple on the group delay specification of the filter. Otherwise said, the ripple on the group delay should be smaller than 5% for every amount of boost [38].

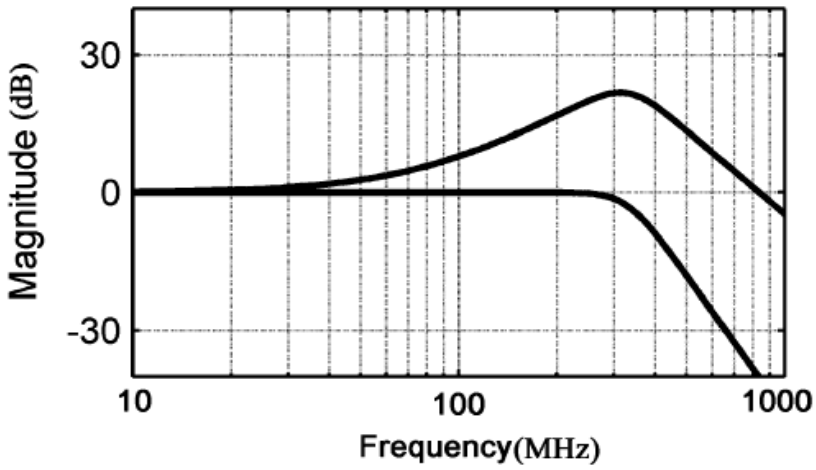


Figure 2.8 Magnitude responses of lowpass filter with and without gain boost [38]

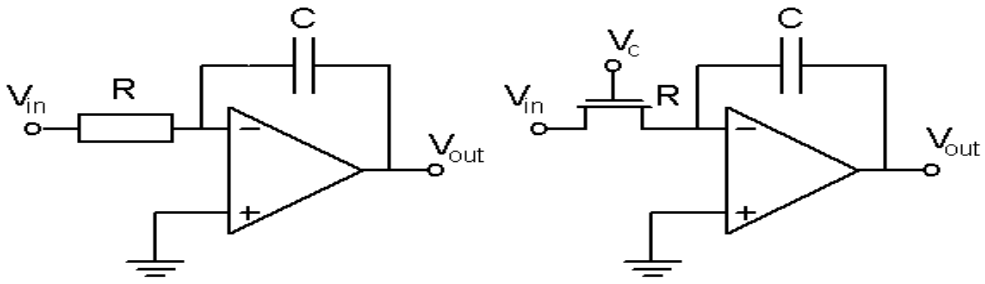
Higher speed higher density data systems require higher gain boost. The maximum gain boost in current practice may be as high as 24dB [49]. The programmable equalization or gain boost is achieved by using a filter function with gain-boost zeros. This feature is typically realized by adding two opposite real axis zeroes into the overall frequency response; in this way it is possible to modify the amplitude response without changing the group delay response. In some of the approaches [32, 36-40, 42, 51, 52] reported in the literature, seventh-order filters have been reported to achieve a flat group delay response up to 1.75*fc*, where *fc* is the 3dB cut-off frequency of the filter. However, instead of using a Bessel filter for a flat group delay response these approaches are mostly based on a 0.05° equiripple linear phase response, which extends the frequency range of the flat group delay response. In the case of Bessel type transfer function the flatness of the group delay response normally degrades around 1.2*fc*. A traditional approach in defining the filter pole constellation when a flat group delay characteristic is needed [1] is based on the above mentioned 0.05° equiripple approximation of the phase. In [40] such a seven-pole constellation, which yields linear phase almost up to 2*fc* was selected. However this scheme had two zeroes on the real axis in the seven-pole constellation thus resulting effectively in a fifth-order roll-off. The placement of these left and right half zeroes was externally controlled and this resulted in a better correction of flat group delay response in the

band of interest, thus helping to equalize somewhat asymmetrical pulses from the media.

2.3 Previous Work in Analogue Filters for HDD Systems

HDD systems have developed rapidly in the last ten years to meet the emerging demands of high performance computing and peripheral devices. The hard disk industry is continually developing read channel chips to push data rates higher, while simultaneously achieving low power and low cost solutions. The main requirements for design of analogue lowpass filters for future generation of read channels are high cutoff frequency (200 to 800 MHz), small group delay variation (5%), high gain boost (20dB), very low power and small chip area. However, designing filters operating at very high frequency (VHF) or ultra high frequency (UHF) in pure digital CMOS is very challenging. Among different methodologies of filter design, the switched-capacitor (SC), MOSFET-C, and OTA-C are the most popular in the literature. The switched capacitor filter allows for very accurate and tunable analogue circuits to be manufactured without using resistors. This is useful for several reasons. The resistors take up a lot of die area and the response shape of the SC circuits can be made to depend on ratios of capacitor values (which can be set accurately). The cut-off frequency of the filter is also precisely determined by the clock frequency. However, SC filters are not well suited to operation at very high frequencies due to the requirement for very high frequency switching clock and associated problems with aliasing, and the need for very fast Op-amps. MOSFET-C filters are extremely widely used for lower-frequency applications where low distortion is important. The MOSFET-C technique was derived from active-RC techniques; in discrete component designs, the useful frequency range of the active-RC filter is limited by parasitic capacitances to frequencies mostly below 1MHz. However, in a fully integrated design, circuit parasitics can be reduced sufficiently to allow satisfactory performance at frequencies of 10MHz or greater. To achieve a filter with tunable cut-off frequency, the resistors of the active-RC design are replaced with MOSFETs operating in the

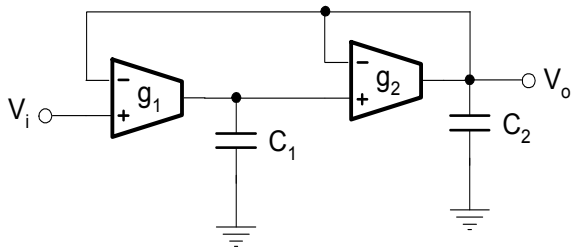
triode region, where the channel acts as a variable resistance which is dependent on the gate and substrate bias voltages. The cut-off frequency and Q of the filter are tuned by varying the gate voltages. A MOSFET used in this way is usually called a MOS resistor. The basic active-RC integrator is shown in Figure 2.9(a). Figure 2.9(b) shows a basic MOSFET-C integrator.



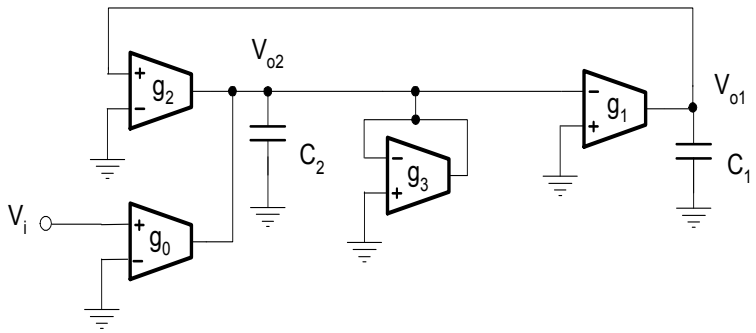
(a) (b)

Figure 2.9 (a) Active-RC and (b) MOSFET-C integrators

Two most popular two integrator loop OTA-C filter structures [1] are given in Figure 2.9. The structure in Figure 2.9(a) is a canonical (minimum number of components) two integrator loop OTA-C filter which consists of two single-loop ideal integrators in cascade. The so-called Tow-Thomas (TT) OTA-C structure in Figure 2.10(b) consists of an ideal integrator and a lossy integrator in a single loop. This biquad is simple in structure, and has low parasitic effects and very low sensitivity (as it is a simulation of a passive RLC resonator prototype) [5].



(a)



(b)

Figure 2.10 Two integrator loop OTA-C filter structures: (a) canonical, (b) Tow-Thomas

The development of HDDs has resulted in lowpass filter cutoff frequency increasing from tens of MHz in the early years to several hundreds of MHz more recently [26-42, 47-59]. However, neither the SC filter nor the active-RC filter is suitable for VHF operation as required by current HDD read channels. Although a few papers have also been published using other techniques, e.g. using the OTA-Op-amp-C technique to reduce parasitic effects [78, 85], the Op-amp performance still limits their working frequency. The OTA-C filter therefore becomes the only solution for modern HDD read channel design due to its open-loop structure.

Due to the requirements of SoC to integrate both analogue and digital circuits, it is currently necessary to design analogue parts using deep sub-micron digital CMOS processes. Among different IC technologies, Bipolar was one of the earliest technologies used in linear phase filter design [26, 27], to provide high-speed performance. Bipolar devices are attractive in terms of high speed, high driving capability and low noise, allowing high-quality analogue performance. Nevertheless, limitations of Bipolar technology include low integration density, high cost, and high power; therefore it is not used for modern HDD systems. BiCMOS technologies have also been used for HDD applications [28-32]; this technology has played a vital part in several SoC designs (e.g., telecommunication circuits). However, existing BiCMOS technology still suffers from low integration density compared to pure CMOS

technologies, although it combines the technical benefits of Bipolar and CMOS technologies. Therefore, for technological reasons (related to low integration and complex fabrication processes) CMOS now has overshadowed Bipolar and BiCMOS for both digital and analogue design. CMOS provides favored characteristics for high density digital integration such as low power, negligible static power dissipation and large noise margins with relatively low cost. However, CMOS devices have a low driving current capability, which is a drawback for high speed applications. Moreover, narrow gate width offers fast speed and low power consumption, but the smaller geometries lead to poorer matching between transistors. Therefore, it is a challenging task to design a high performance lowpass filter in HDD systems by using pure CMOS technology. This thesis will therefore focus on CMOS OTA-C filters only, although discussions such as filter structures are also applicable to other IC technologies and filter circuit techniques.

A brief summary of some of the previously reported work has been shown in Table 2.3.

Table 2.3 Comparison of other linear phase lowpass filters

	Type	Process	f_c range (MHz)	f_c accuracy	Boost range	Boost accuracy
De Veirman [26]	7^{th}-order 0.05^0 equiripple linear phase	Bipolar	2-10 B: 6-27	±5%	0-9dB	±0.5dB
Laber [28]	6^{th}-order Bessel	1.5μm/4GHz BiCMOS	4.7-20.3 B: 14-55	±5%	0-10dB	±0.5dB
Chiang [42]	7^{th}-order 0.05^0 equiripple	2μm CMOS	5-20 B: 10-47	N/A	0-3dB	±0.5dB

	linear phase					
Mehr [40]	7^{th}-order 0.05^0 equiripple linear phase	0.6μm CMOS	6-43 B: 15-105	< ±10%	0-12dB	±1dB
Dehaene [38]	7^{th}-order 0.05^0 equiripple linear phase	0.7μm CMOS	B: 5-50	< ±10%	0-13dB	N/A
Rezzi [32]	7^{th}-order 0.05^0 equiripple linear phase	0.7μm BiCMOS	B: 7-50	N/A	0-13dB	±1dB
Rao [27]	7^{th}-order 0.05^0 equiripple linear phase	0.29μm BiCMOS	10-100 B: 30-235	±5%	0-13dB	N/A
Martinez [39]	7^{th}-order 0.05^0 equiripple linear phase	0.35μm CMOS	160-220	N/A	N/A	N/A
Martinez [41]	4^{th}-order 0.05^0 equiripple linear phase	0.35μm CMOS	550	≤10%	N/A	N/A
Bollati [33]	8^{th}-order 0.05^0 equiripple	0.25μm CMOS	30-120	N/A	6-14dB	N/A

	linear phase					
Dosho [52]	7^{th}-order 0.05^0 equiripple linear phase	0.25μm CMOS	B: 80-200	N/A	0-13dB	N/A
Gambhir [49]	4^{th}-order Butterworth	0.18μm CMOS	350	15%	0-24dB	±0.5dB

	Group delay Ripple	THD	Total output noise	DR	FOM
[26]	<2% @ f <2f_c	<-40dB (V_{id} = $2V_{pp}$ with an input attenuator)	2.5mV_{RMS} B: 4mV_{RMS}	49dB B: 45dB	12.6
[28]	<2% @ f_c/6<f <f_c	<-52dB (V_{od} = $2V_{pp}$)	2mV_{RMS}	N/A	117
[42]	≤5% @ f ≤2f_c	<-47dB (V_{id} = $1V_{pp}$ @ 1MHz)	N/A	N/A	390
[40]	<2% @ f <1.75f_c	<-40dB (V_{id} = 640mV_{pp} @ 2MHz, no B, any f_c setting)	N/A	>60dB	763
[38]	<2% @ f_c /5< f <1.5f_c	<-40dB (V_{id} = 200mV_{pp})	3mV_{RMS}	N/A	154
[32]	<2.5% @ f_c/10< f <1.5f_c	<-40dB (V_{id} = 500mV_{pp} @ 24MHz input, f_c = 32MHz)	650μV_{RMS}	52dB	263

[27]	<5% @ $f \leq 2f_c$	<-46dB (V_{id} = 100mV_{pp} @ 30MHz input, f_c = 65MHz)	N/A	48dB	256
[39]	<3% @ f_c /5< f <1.2f_c	<-46dB (V_{id} = N/A)	N/A	51dB	1628
[41]	<15% @ $f \leq f_c$	<-40dB (V_{id} = N/A)	N/A	N/A	3025
[33]	N/A	<-40dB (V_{od} = 200mV_{pp} @ 120MHz input, f_c = 120MHz)	N/A	B: 45dB	250
[52]	≤5% @ f <1.5f_c	<-40dB (V_{id} = 800mV_{pp} @ 200MHz input, f_c = 200MHz)	562μV_{RMS}	N/A	361
[49]	<15% @ f_c /5≤ f ≤1.1f_c	<-40dB (V_{id} = 315mV_{pp} @ 1MHz input, f_c = 100MHz)	BW = 500MHz B: 300μV_{RMS}	B: 55dB	3324

Notes: f_c - cut-off frequency, B - boost, V_{id} - differential input voltage, V_{od} - differential output voltage, N/A - not applicable, BW – bandwidth, FOM- Figure of merit.

These designs range over several different process geometries. In order to compare them in a meaningful way, a figure of merit (FOM) is used in Table 2.3 [41]. The cut-off frequency f_c is in general in the range of 2 – 350MHz. As stated, there is a requirement in the hard disk industry for even higher frequencies for higher data rates.

It can be seen from Table 2.3 that pulse equalizers in the read channel are normally realized as high order lowpass filters. Bessel filters and 0.05° equiripple linear phase responses are mostly used.

2.4 Filter Design Considerations for Read Channel OTA-C Filters

As mentioned before, VHF/UHF filter design is one of the major challenges in this work. For the HDD read channel filter designs described in Chapters 3 and 4, a very high cut-off frequency is a prime target. The high cut-off frequency will enable the high data rates required in a state-of-the-art HDD. As a rule of thumb, a filter with a cut-off frequency of at least 500 MHz will be required for data rates up to 2*Gbp/s*[40, 41, 45]. As well as specifying the system bandwidth, selecting the correct transfer function, including the equalization feature, the filter circuit architecture, and the OTA design requirements are important tasks for such a filter.

2.4.1 Group Delay Response

One of the most important specifications of the analogue pulse equalizer is the ripple on the group delay. It should be generally smaller than 5% [26-61]. The group delay ripple is defined as the maximum variation of the group delay relative to the nominal average group delay in a certain frequency band. They are given below.

Nominal group delay:

$$tgr\_nom = \frac{Max\ [tgr(f)] - Min\ [tgr(f)]}{2}$$

Group delay ripple:

$$ripple = \frac{Max\ [tgr(f)] + Min\ [tgr(f)]}{2tgr\_nom} \tag{2.1}$$

Where *Min* and *Max* are taken over the range $0.2fc < f < 1.7fc$, *fc* is the filter's cut-off frequency, and *tgr(f)* is the group delay.

Therefore, a 0.05° equiripple linear phase transfer function was selected. Analyzing a Chebyshev approximation of a magnitude function reveals an advantage in that the

permitted magnitude error is uniformly distributed over the passband rather than increasing monotonically towards the corner of passband as in the maximally flat response, leading to a smaller maximum error within the passband. When considering possible delay approximations for the HDD filter application, similar advantages are offered if we develop a filter with an equiripple delay, rather than maximally flat (Bessel-Thomson) approximation. Figure 2.11 shows the performance we hope to obtain for a desired specific delay with these two different 5th order responses. As the figure illustrates, the 0.05° equiripple linear phase approximation achieves a delay error within a limit of 5% over a significantly wider total bandwidth than the maximally flat approximation of the same complexity.

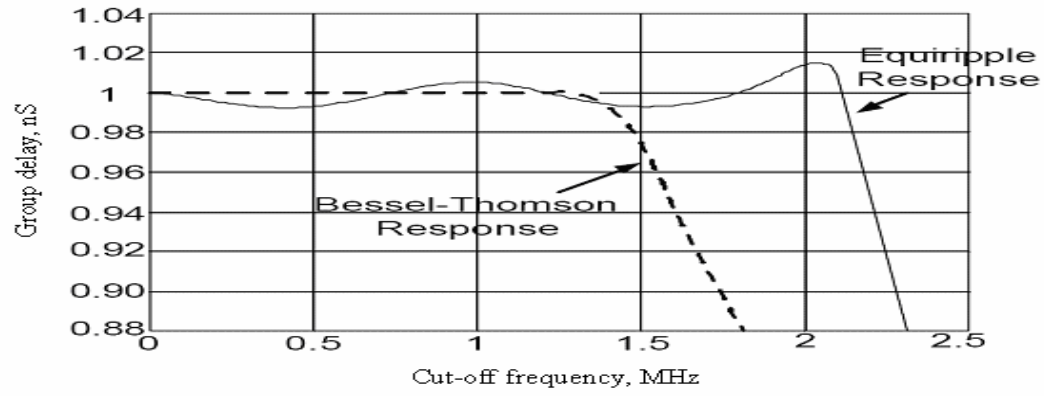


Figure 2.11 Comparison of group delay of Bessel-Thomson and Equiripple approximations

2.4.2 Transfer Function of the Filter

A detailed mathematical analysis of the 0.05° equiripple linear phase transfer function is given in literature [7, 8]. Analyzing the generic transfer function of a 0.05° equiripple linear phase transfer function,

$$T_E(s) = \frac{E(0)}{E(s)} = \frac{a_0}{s^n + a_{n-1}s^{n-1} + \cdots + a_1 s + a_0} \tag{2.2}$$

We can impose the condition that the group delay approximates a constant value with uniform error over the desired bandwidth. Unfortunately a closed form solution for the equiripple delay transfer function has not been found. Since constant group delay is equivalent to linear phase, we can write the equation of phase as a linear

function and assume a sinusoidal ripple for ease of analysis

$$\theta(\omega) = -D_0\omega - \Delta\theta \sin(\omega T) \tag{2.3}$$

The group delay is then given by:

$$D_E(\omega) = -\frac{d\theta}{d\omega} = D_0 + \Delta\theta \cdot \pi/180^\circ \cdot T \cdot \cos(\omega T) \tag{2.4}$$

where the θ was converted into radians. T is the period of the ripple; it is approximately equal to the constant delay bandwidth divided by $n/2$, n being the degree of the function $T_E(s)$ determine the polynomial $T_E(s)$ differential equations can be employed. The phase of equation (2.3) has exactly n locations where the slope equals D_0 (some constant group delay). The delay error is given by the following equation:

$$\Delta D = 2T \cdot \Delta\theta \cdot \frac{\pi}{180^\circ} \tag{2.5}$$

It is twice the ripple width and is independent of n. The delay error is proportional to the phase error as indicated by equations (2.4) and (2.5). For $\Delta\theta$=0.05° the error is ΔD≈0.015. However the bandwidth ω_E over which the delay error ΔD remains constant and stays within the design specifications increases with n. Based on the above discussion we can then decide what order of filter response will be implemented. Since the primary target of the design is to reach high cutoff frequencies in the range of 500-800MHz, the number of poles plays a very important role. Ideally, a higher order filter has maintains an accurate group delay response over a greater bandwidth than a lower order design. However, the number of OTAs in the system is proportional to the number of poles. Since each OTA contributes some phase error to the overall response, OTAs with lower phase error are required to achieve an accurate response in a higher order filter The required cut-off frequency of each OTA can become very high (of the order of GHz in the case of a seventh-order filter). Moreover, in order to achieve higher filter cutoff frequency, larger OTA transconductance and smaller grounded capacitance are needed, increasing the power consumption and chip

area. This prompts us to choose a relatively low order lowpass filter, such as fourth- or fifth-order.

Apparently, a lower order filter can minimize the power consumption, chip area and the design effort required. Unfortunately, the group delay ripple can not be maintained over as wide a bandwidth as in a higher order design. In Figure 2.11, fifth- and seventh-order equiripple linear phase filters are simulated using idealized OTAs. It can be seen from Figure 2.12 that the group delay response of the 7^{th} order filter remains flat over a wider bandwidth.

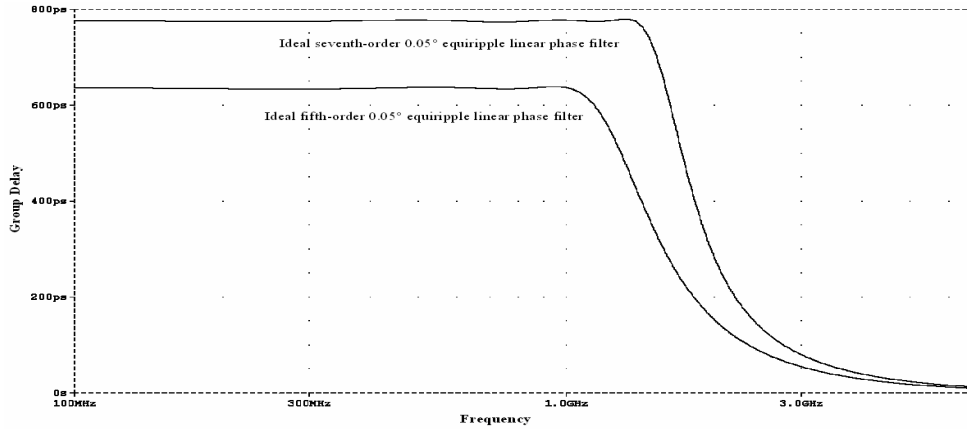


Figure 2.12 Comparison of group delay ripple of ideal seventh- and fifth-order 0.05° equiripple linear phase approximation

2.4.3 Filter Architectures

Filter structure plays a very important role in analogue filter design. Among different filter topologies, the cascade, LC ladder simulation, and multiple loop feedback (MLF) are the most popular in the literature. The cascade topology is possibly the most popular due to simplicity in design and tuning. However, the sensitivity of cascade filters is high, and increases as the filter order increases. LC ladder simulation based filters have low sensitivity, but the design methodology is relatively complex [1, 2, 5, 7, 8, 10, 51, 52, 65, and 111]. In some implementations, LC ladder simulations contain some floating capacitors, which can seriously affect group delay ripple due to parasitic effects at UHF/VHF. The MLF methodology is

simple and it has sensitivity as low as LC ladder simulations. Therefore, it has received considerable attention [1-4, 36, 37, 42-44, 53-62, 105-108, and 117-121]. Moreover, as discussed previously, the parasitic capacitance can dominate the total nodal capacitance at UHF/VHF. The use of only grounded capacitors in MLF topologies can minimize the parasitic effects, since the parasitic capacitances can be absorbed into these. This is very important in achieving high cut-off frequencies for modern fast HDD application. Any of these filter design methods can be used for linear phase filter design. However, additional circuits may be needed to implement gain boosting, which is realized by the addition of real zeros to the basic low pass response.

Several topologies have been proposed to realize these symmetric zeros. Many of them make use of additional circuits that require a large amount of power to keep the parasitic poles out of the band of interest. The cascade topology can be utilized by including additional biquads with real zeroes [33, 38-41, 46-50], or linear phase biquads cascaded with a FIR filter to produce zeroes, [48] or cascaded biquads with cross-stage feed-forward connections [27, 49]. However, the LC ladder simulation topology cannot directly realize real zeroes. In the MLF circuit using feed forward input or output network structures, the zeros can be realized by adding additional OTAs to the basic lowpass structure.

The well known leap frog (LF), follow the leader feed back (FLF) and inverse follow the leader feedback (IFLF) MLF configurations have also been used for HDD application. Comparisons of cascade, LF, and IFLF filters can be found in the literature [43, 54, and 61]. The FLF and IFLF topologies may be more sensitive to parasitics due to their global feedback paths. The LF based structure has been proved to have the best phase response. Therefore, linear phase lowpass filters based on voltage-mode LF structure have been used for HDD application [36, 37, and 54]. Since analogue signal processing in the current domain can offer advantages for many applications, including simplicity, high frequency operation and wide dynamic range, researchers have paid much attention to current-mode CT filters [104-108, 118]. For

current-mode signal processing and filtering, circuits are normally based on current integrators, current amplifiers, and current feedback, with current inputs to circuit nodes and current outputs from OTA output terminals. Design formulae for the current-mode FLF filter configuration has been proposed in [107]. However, design formulae for current-mode LF configurations have not previously been proposed in the literature. Therefore, we will propose the design formulae of current-mode LF configuration in Chapter 4.

2.4.4 Filter Circuits and Tuning

Although the above filter structures may be suitable for any circuit implementation, due to high-speed and economic requirements, CMOS OTA-C filters are the only suitable type for implementation of high-speed CT filters.

From the viewpoint of the analogue designer, CMOS processes, whilst yielding active devices capable of excellent high-speed performance, are mediocre from the point of view of component value accuracy. Each type of component is fabricated during several process steps, each of which contributes variability to the final component value. Typically, initial component tolerances of the order of several percent to tens of percent can be expected. It is interesting to note that, in spite of the great strides made in semiconductor technology during the past few decades, component tolerances have improved little. It is possible to fabricate accurate on-chip components, but the need for extensive additional processing makes this impractical for applications where high yield and low cost are of paramount importance. At high frequencies, parasitic capacitances in the circuit layout are an additional source of inaccuracy in component values, and have more poorly defined values than fabricated capacitors. While grounded capacitors may readily absorb parasitic capacitance at lower frequencies, at UHF/VHF parasitic capacitance may dominate the total capacitance, and indeed parasitic capacitances may be used as filter capacitances in the GHz range. The pole and zero frequencies of the filter are dependent on the values of at least two different types of component, in the case of gm-C filters transconductance and capacitance,

each of which is subject to uncorrelated tolerance variations. Therefore, tolerances on the initial cut-off or centre frequencies of the filter of 50% or more can be expected.

In principle, the desired filter response could be obtained by trimming components on the die after fabrication. With active laser trimming, the total dependence on the fabrication manufacturing processes can be eliminated. However, this is impractical for economic reasons. While in standard IC processing, a large number of chips are processed in parallel, simultaneously, on a single wafer. This is a fundamental factor that allows production of complex ICs at very low cost. On the other hand, a post-fabrication trimming process would have to be performed on each die individually, adding significantly to test times and so to production cost. Also, even if accurate initial values could be achieved, the components on the IC are subject to further substantial variations in value due to the effects of ageing and environmental variables, in particular temperature.

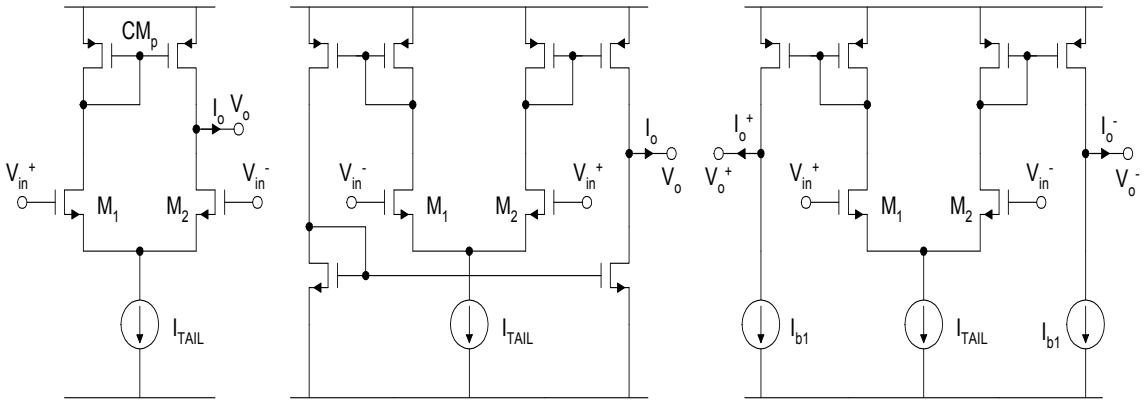
Therefore, an automatic on-chip tuning system is normally needed. For the HDD read channel application, cut-off frequency tuning is the main requirement [2, 8, 38-40, 51, 52]. Q tuning is not generally necessary for HDD read channel filters due to their low design Q. However, both frequency and Q tuning may be needed for analogue transceiver filter design. The most popular tuning method used for lowpass filtering is the master-slave method [38-40, 50-52] based on phase locked loop [38-40] or frequency locked loop [50-52]. It is noted that the design of tuning system is excluded in this thesis, although it is important for actual implementation.

2.5 OTA Design Considerations for Read Channel OTA-C Filters

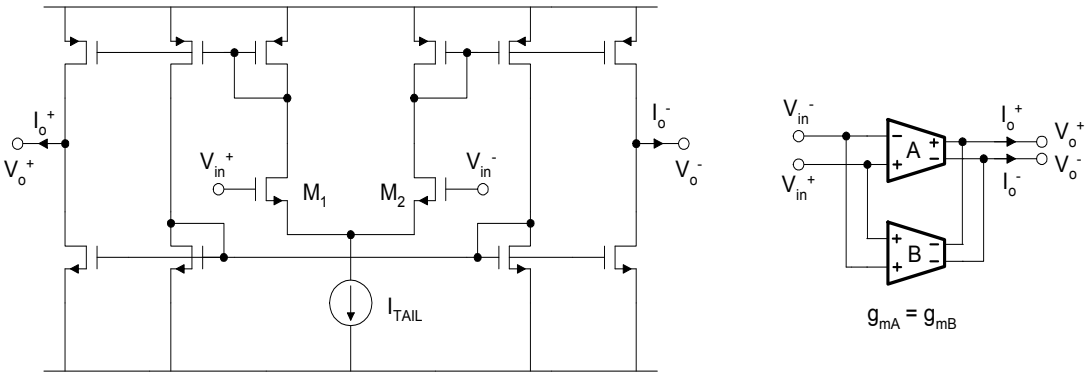
For UHF/VHF applications, the voltage to current transducer must be able to operate properly at high frequencies. Although the use of small load capacitors, 0.2-0.4 *pF*, would be desirable, parasitic capacitance is typically larger than these values [41]. Also, in a real filter, several OTAs are sharing the same node, increasing the total parasitic capacitance at that node to the range of 0.4-0.8 *pF*. Therefore, small

signal transconductances of around 0.8 *mS* (for a 100 *MHz* pole) and up to 8 *mS* (for a 1 *GHz* pole) are required. The implementation of large transconductance requires the use of wider transistors and larger tail currents. The use of small transistor lengths pushes the parasitic poles to higher frequencies, but the DC gain of OTA is reduced and mobility degradation effects become more severe. On the other hand, the use of large drain currents reduces the available DC gain even further and increases the power consumption. Another important design aspect is the effect of the OTA excess phase at the filter cut-off frequency, due to the OTA output resistance and the parasitic poles and zeros. Very often, large gate-source voltages are desirable in order to improve OTA linearity, but the low supply voltages limit this possibility.

Among different OTA topologies, the pseudo-differential and fully-differential topologies are the most commonly used. Figure 2.13(a) shows a basic differential (unbalanced) OTA with a simple current mirror and a single output. In fact, it is the well known simple single differential pair OTA. Note that the structure of the circuit is non-symmetrical and thus generates excessive noise. The balanced version (symmetrical) of the OTA is shown in Figure 2.13(b) with three current mirrors and a single output. Figures 2.13(c) and (d) show fully-differential (fully symmetrical in architecture) OTAs without common-mode feedback (CMFB) and with inherent common-mode feed forward (CMFF), respectively. Note that the OTAs in Figure 2.13 do not have very high DC gain. To obtain higher DC gain, cascode structures may be used as the output stage of the OTA [110].



(a) (b) (c)



(d) (e)

Figure 2.13 Differential CMOS OTAs: (a) simple differential, (b) balanced, (c) fully-differential (without CMFB), (d) fully-differential (with inherent CMFF), and (e) pseudo-differential OTAs

The architecture of the pseudo-differential OTA shown in Figure 2.13(e) is suitable for LV/LP operation. The circuit consists of two parallel-interconnected transconductors (labeled A and B) of equal DC transconductances. The transconductor A is a pseudo-differential transconductor, which can be implemented using two single-input transconductors. The configuration of the transconductor A requires a CMFF circuit to reduce its common-mode signal. The CMFF circuit can be realized using an additional, non-differential input and dual (equal) output transconductor (transconductor B). Topologies based on this pseudo-differential pair have been proposed in [30, 35]. This approach can be very efficient in terms of power consumption. The pseudo-differential OTA is based on two independent inverters without a tail current source. Avoiding the voltage drop across the tail current source, this structure can achieve wider input range and make the architecture attractive for reduced power-supply applications. However, removing the tail current source significantly increase the common-mode gain. No analogue circuit is totally immune to supply noise; any signal or noise on the supply lines will couple into the signal path through the stray capacitances and gain of the bias network and be amplified by the active circuitry on the die. This power supply noise degrades the overall noise performance of the OTA. A high power supply rejection ratio (PSRR) is required

because, in mixed-signal SoC environments, digital switching noise signals will be injected into the analogue circuitry through the power supply rails, degrading the performance of the analogue circuits. Therefore, topologies based on fully differential pair have been widely used for HDD applications due to better dynamic range, distortion performance, and noise rejection.

Among fully differential OTA structures, cross-coupled [36, 37, 42-44] and source degeneration [33, 38-41, 50-52] based OTAs are commonly used, which are shown in outline in Figure 2.14, 2.15 respectively.

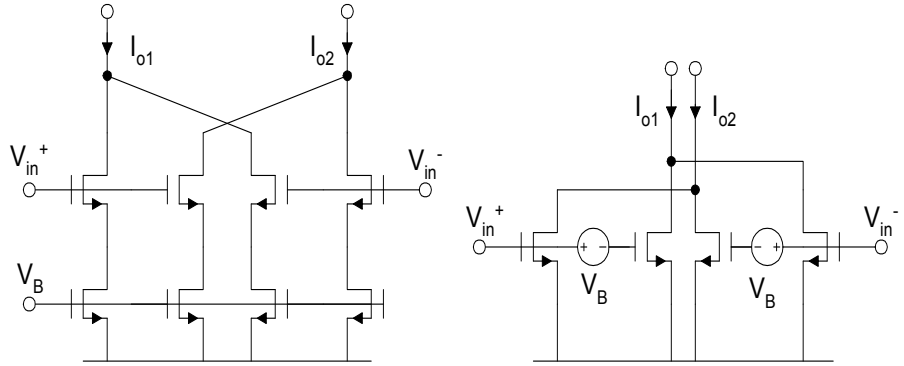


Figure 2.14 Implementations of the cross-coupled OTA

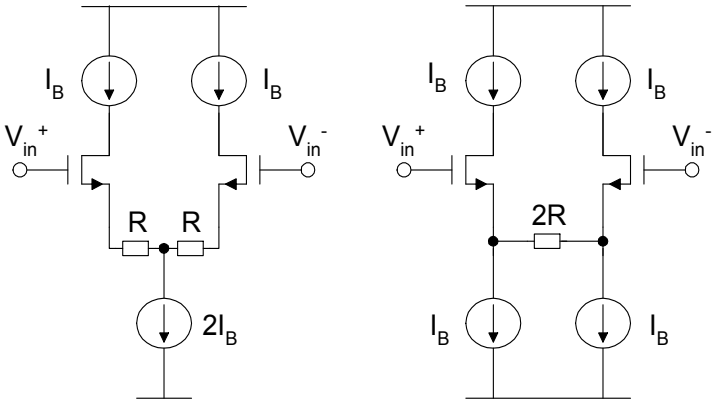


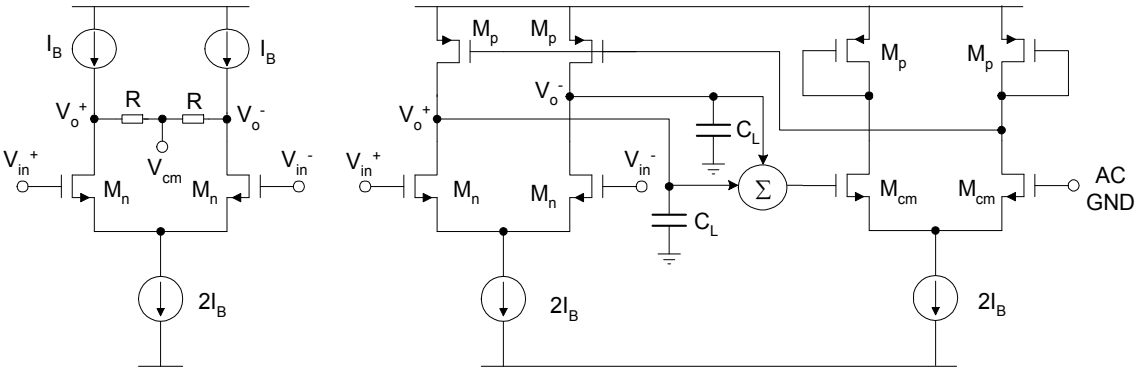
Figure 2.15 Two possible topologies of source degeneration techniques

In the source degeneration technique, non-linearity is reduced by making transconductance primarily dependent on linear source resistors. One drawback of the source degenerated OTA is that the transconductance tuning range of the OTA therefore is limited; the total transconductance is also reduced, which depends on the sizes of source degenerated transistors. On the other hand, although the cross-coupled

OTA structure can also reduce nonlinearities [42-44, 54], it is not usually used because the superior linearity is achieved at the expense of increased power consumption and noise. Currently, source degeneration technique attracts more attention. In [40], a fully-differential OTA is proposed. This cell is designed to have a significant size for improved matching of V_T. Moreover, the V_{GS} of input differential pair is maintained constant by using feedback loops which force constant current feedback to the input differential pair. However, this structure adds two internal nodes which significantly affect the phase response of the OTA and it is hard to maintain low group delay ripple in the filter at high frequency. Another OTA based on source degeneration topology is presented in [51]. In [51], a two-input OTA with capacitive loading uses a folded-cascode structure to obtain high output impedance. A low output impedance reduces the DC gain of the OTA and also produces phase errors. This is especially true for designs using small process geometries. Fortunately, lowpass filters for HDDs are generally low-Q applications, so a modest DC gain of 20dB is sufficient to realize tolerable gain and phase errors. Folded-cascode or telescopic architectures provide high DC gain and good noise rejection, but again for high-frequency designs the non-dominant poles due to internal nodes degrade the filter phase response. Also the cost of lower input voltage range, or greater supply voltage, and greater chip area must be paid. In order to achieve high frequency with low power consumption, simpler single-stage OTAs are preferred. Improved filter response can be expected due to absence of internal nodes. Also, single-stage OTAs reduce power consumption and area. The OTA proposed in [39] uses complementary differential pairs with source degeneration transistors to increase the overall power efficiency. The frequency response of this OTA is very good due to the absence of low-frequency parasitic poles. Using the similar OTA in [41], 550MHz cut-off frequency can be achieved with only 140mW power consumption. However, the DC gain is relatively low, even for the fabricated chip using a 0.35μm process. The effects may become even more severe when using deep sub-micron processes. The tuning range of the OTA is also small. Considering the tuning requirements of HDD applications, it is not necessary to use

either capacitor arrays or transconductor arrays to tune the cut-off frequencies of the lowpass filter. Transconductance tuning alone can achieve adequate tuning range. Tuning transconductance is normally achieved by changing DC bias or supply voltage, both of which are strongly related to power consumption. Moreover, the tuning range of most OTAs is less than 1:2. However, the overall filter tuning range required is 1:2 at least. Therefore, new techniques must be proposed in order to fulfill this requirement. In [33], a 1:4 tuning range is achieved by exploiting a dual-loop control over a source degeneration based differential pair. However, the use of a large number of source degeneration transistors switched on or off occupies more area, particularly where larger transconductance is required. As mentioned before, it is desirable to only use simple OTA structures in order to achieve better high frequency performance for next generation HDD analogue filter solutions.

Fully differential filter circuits are ubiquitous due to their improved noise rejection. However fully-differential circuits usually require a common-mode feed back (CMFB) circuit to stabilize their DC operating point, and reduce common-mode gain in the circuit. In most fully-differential OTA-C filters [9-11, 110], an associated CMFB circuit is included to overcome this problem, either as an integral part of the OTA design, or acting on the overall circuit. The basic concept of the CMFB loop is shown in Figure 2.16 [110]. Figure 2.16(a) illustrates a basic differential OTA with a common-mode detector implemented using two identical resistors. Figure 2.16(b) shows a conceptual implementation of the CMFB loop. The sensed common-mode signals are summed, compared with the common-mode reference (AC ground), and the resultant current is fed back to the OTA to adjust its bias current. The basic design constraints of a CMFB circuit are described in [110].



(a) (b)

Figure 2.16 CMFB basic circuit concept: (a) basic common-mode detector and (b) CMFB implementation

2.6 Conclusions

Design considerations for high performance analogue lowpass filters for HDD systems have been presented in this chapter. The choice of OTAs, filter order, filter approximation, and filter architecture by considering their advantages and disadvantages have been addressed. Design trade-offs in relation to power consumption, speed, group delay ripples and large tuning range have been discussed. Currently, filter architectures used to implement HDD analogue lowpass filters are mainly based the cascade structure. Recently, the well-known MLF structure has also been proposed for HDD read channel applications. In [36], a single-ended LF structure has been used, but it is not suitable for state-of-the-art mixed-signal processing. Therefore, a fully-balanced form has been proposed in [37]. The power consumption of designed lowpass filter is high for modern HDD systems which use the cross-coupled type of OTA. The latest research shows that the current-mode LF and FLF architectures can also achieve high speed with reasonable power consumption [57, 59]. For the future, the high efficiency solutions for read channel chip are much in demand. The design considerations presented in this chapter serve as the guidelines for the multiple loop feedback OTA-C filters for HDD read channels described in the next three chapters.

3. Design and Simulation of Linear Phase MLF FLF and IFLF OTA-C Lowpass Filters for HDD Read Channels

3.1 Introduction

Theory and design methods of multiple loop feedback (MLF) operational transconductance amplifier (OTA-C) topologies were developed in [1-4, 42, 43, 105-107, 117-126]. In recent years, the MLF follow-the-leader-feedback (FLF) and inverse-follow-the-leader-feedback (IFLF) OTA-C filter configurations have attracted attentions due to simple design methodologies. The voltage-mode MLF IFLF configuration has been used for computer hard disk drive (HDD) read channels since 1996 [42]. However, the cut-off frequency of voltage-mode MLF IFLF filters is relatively low. Moreover, current-mode MLF FLF configurations have not been used for HDD read channels in the literature.

For the solution of next generation HDD read channels, the power consumption needs to be further reduced. Although the easiest way to reduce the overall power consumption is to use low order filters instead of high order ones [41, 49, 78, 85, 103], the overall filter performance is degraded as the filter order decreases. Using reduced supply voltage can also certainly reduce total power consumption of circuits, but most specifications of the continuous-time filter rely on supply voltage strongly. In particular, the speed of a filter is limited by reduced supply voltage severely. On the other hand, it is challenging to design a FLF or IFLF linear phase filter, although the FLF and IFLF structures have been used to optimize the filter performance and power consumption for HDD read channels [42, 59]. This is because they have a main intrinsic drawback in that their global feedback loops introduce hard-to-minimize phase errors, which severely affect the filter group delay responses. Therefore, our research focuses on design of linear phase FLF and IFLF filters in this chapter. The target specification for the filter is given in Table 3.1.

Table 3.1 Design targets of the IFLF and FLF filters for computer HDD read channel

Specification	Cut-off frequency	Gain boost	Group delay ripple	Dynamic range	Power consumption
Target	300MHz	10dB	5%	35dB	100mW

In the next section of the chapter, Section 3.2, the multiple output and multiple input OTAs are designed and simulated for filter implementation. The synthesis of current-mode FLF filters with input distribution and output summation is presented in Section 3.3, where both current-mode seventh- and fifth-order 0.05° equiripple linear phase FLF OTA-C lowpass filters are designed using proposed two input four output OTA. The seventh-order voltage-mode 0.05° equiripple linear phase MLF IFLF OTA-C lowpass filter is also designed and simulated by using four input two output OTAs in Section 3.4. In Section 3.5, the detailed simulation results of all presented filters are given. Finally, discussion and conclusions are provided in Section 3.6.

3.2 Transistor-level OTA Design

The OTA is the dominant building block for high frequency active circuit design in use today. The frequency and linearity characteristics of an OTA directly impact on the filter performance. In this section, we describe the development of two input four output and four input two output OTAs.

3.2.1 Single Stage OTA Design

A new OTA which takes advantage of the fully-symmetrical structure is presented. The circuit implementation of the simplified proposed fully-symmetrical OTA is shown in Figure 3.1. The presented structure uses a differential pair in the input stage. The output stages consist of four current mirrors. Instead of mirroring the output current to the other side of the circuit, then subtract with another output current to produce the differential output current. The output stages of the proposed OTA act as buffer. The output current can be taken directly from each side.

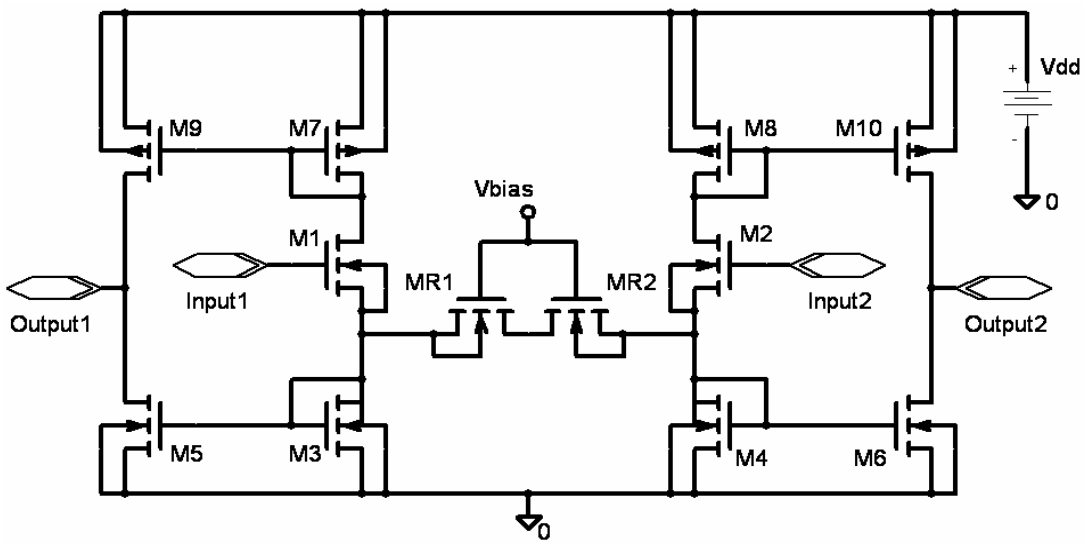


Figure 3.1 Fully-balanced two output OTA

The tail current source is taken over by a pair of current mirrors. The input stage currents are differentially mirrored through P–type current mirrors $M_{9,10}$ and N–type current mirrors $M_{5,6}$ to the outputs. As we can see that the gate voltages of M_{R1} and M_{R2} are connected to be biased with a control voltage source V_{bias}. In order to shift the poles to higher frequencies and obtain the large transconductance, the channel length used for these devices is the minimum length allowed by the process. The M_{R1} and M_{R2} could be connected either in serial or in parallel. It depends on what kind of purpose the OTA is used for. In order to increase the total transconductance value, the widths of the two input stage transistors can be designed to be quite small. To optimize the power consumption, parasitic effects and high frequency response, the triode transistors should be connected in parallel. If a large tuning range is needed, the triode transistors should be connected in serial.

3.2.2 Multiple Output Multiple Input OTA Design

The presented two input four output OTA is shown below in Figure 3.2; the sources of the input transistors are connected to their substrate, which is a common P–well to reduce body effects. The presented structure uses two parallel differential pairs in the input stage. The output stages consist of eight current mirrors. The input stage currents are differentially mirrored through P-type current mirrors $M_{9,11,12}$, $M_{8,10,13}$

and N-type current mirrors $M_{14,\ 16,\ 18}$, $M_{15,\ 17,\ 19}$ to the outputs. Assuming matching between transistors, the output differential current $I_{out} = I_{output1} - I_{output4} = I_{output2} - I_{output3}$. The OTA uses two series connected MOS transistors M_{R1} and M_{R2} in triode region as source degeneration resistors. The gate voltages of M_{R1} and M_{R2} are connected to the separate source followers M_6 and M_7 biased with a control current I_1, so that both DC level shifts are identical, and tuning is obtained via I_1 without disturbing the bias current of the input stage.

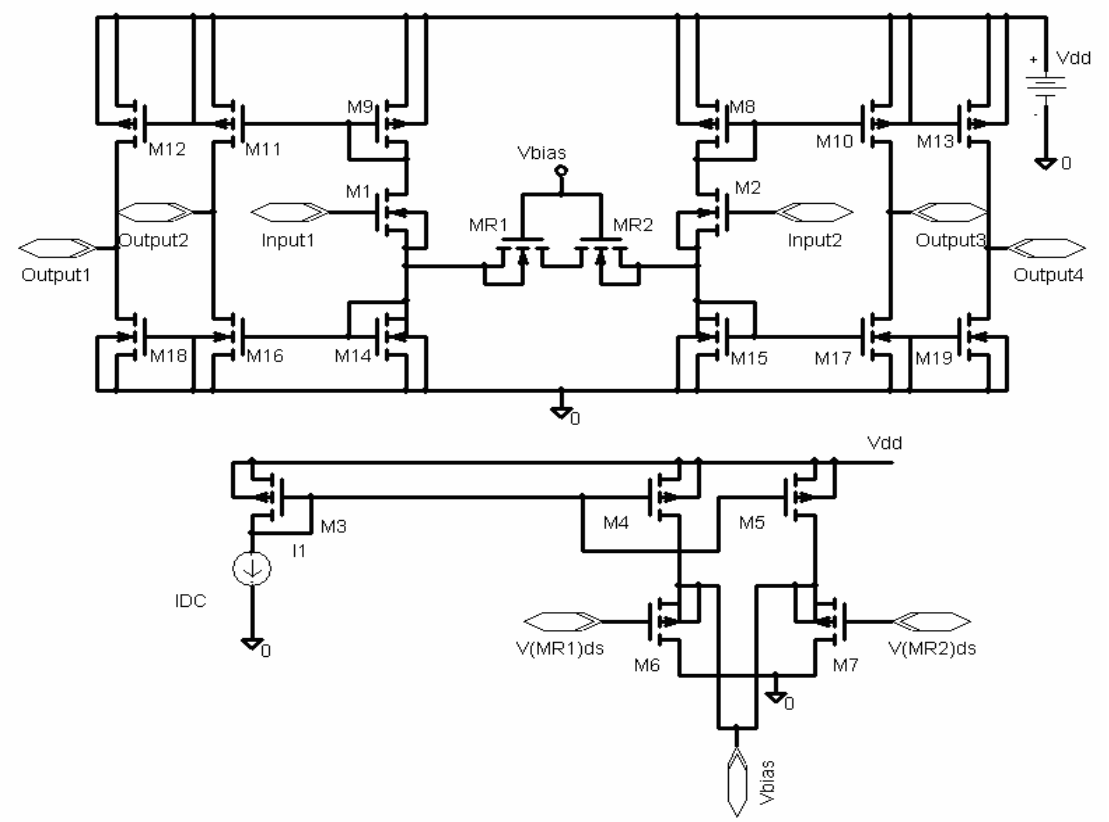


Figure 3.2 Fully-balanced two input four output OTA with bias circuit

The channel length used for these devices is the minimum length allowed by the process and the channel widths are listed as:

Table 3.2 The width of the transistors in Figure 3.2

M_1–M_3	M_4, M_5	M_6, M_7	M_8–M_{13}	M_{14}–M_{19}	M_{R1}, M_{R2}
15μm	30μm	10μm	25μm	9μm	90μm

The drain current of MOS transistors M_{R1} and M_{R2} in triode region is given by:

$$I_{R1,2} = K[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (3.1)$$

where $K=0.5\mu_n C_{ox}(W/L)$ is the N–type transconductance parameter, and μ_n, C_{ox}, W and L are mobility, oxide capacitance per unit area, channel width and length, respectively. Then:

$$I_{out} = I_{output\ 1} - I_{output\ 4} = I_{R1,2} - (-I_{R1,2}) = 2I_{R1,2} \quad (3.2)$$

By substituting (3.1) into (3.2) we get:

$$I_{out} = 2K[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (3.3)$$

Assuming deep source degeneration, which is $2V_{DS} \approx V_{id}$ and $V_{DS} << V_{GS}-V_T$, we have:

$$I_{out} \approx K[(V_{GS} - V_T)V_{id}] = g_m \cdot V_{id} \quad (3.4)$$

Where $V_{id} = V_{input1} - V_{input2}$, V_{id} is the differential input voltage and g_m is the DC transconductance of the MO-OTA given by:

$$g_m \approx K \cdot V_B \quad (3.5)$$

where $V_B=V_{GS} - V_T$. From equation (3.4) and (3.5), we can see that the MO–OTA exhibits a linear V–I characteristic with the assumptions made. Equation (3.5) shows that the transconductance value can be controlled by varying the bias voltage V_B. The bias voltage V_B can be adjusted by the bias current source I_1. Thus, the allowed values of I_1 (V_B) determine the achievable transconductance tuning range. However, in practice, second-order effects such as body effects, mobility reduction, and channel length modulation will degrade the V–I function of the MO–OTA. For high frequency applications the second order effects are severe, therefore often in implementation, the bulks/substrates of most transistors in Figure 3.2 are tied to ground or V_{DD}, apart from the four input stage transistors. For this case, the threshold voltage of $M_{1,3}$, $M_{2,4}$ will be modulated which results in so called body or threshold modulation effects. The threshold voltage of an NMOS transistor is defined by

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) \tag{3.6}$$

Where V_{T0} is the threshold voltage with zero bias, γ is the body/bulk polarization factor or bulk threshold parameter, ϕ is the strong inversion surface potential and V_{BS} is the bulk source voltage [9, 112].

With the mentioned threshold modulation effect for Figure 3.2, using equation (3.6) the modified I_{out} can be shown as

$$I'_{out} = g'_m V_{id} \tag{3.7}$$

Where $g'_m = 2K(V_{GS} - V_{T0} - \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}))$ is the modified DC transconductance of the OTA. There is an error caused by $\Delta V_T = \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$ in g_m'. Thus the bulk effects cause non-linear behaviors in g_m with respect to V_{id}. In practice, thinner gate oxides are recommended to minimize the body effects as γ is decreased with a smaller oxide thickness at the expense of increased mobility reduction. The first-order model of mobility reduction or degradation in MOS transistors is given by

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} \tag{3.8}$$

where μ_o is the zero-field mobility of carriers, $\theta = 1/t_{ox}E_{CR}$ is the coefficient of the effect of the electric field on the mobility, t_{ox} is the gate oxide thickness and E_{CR} is the critical field. An ideal square-law MOSFET has a resistance R_{sx} in series with the source. The R_{sx} can be expressed as [9],

$$R_{sx} = \frac{1}{E_c \mu_0 C_{ox} W} \tag{3.9}$$

Therefore, the θ can also be modelled as $\mu_0 C_{ox}(W/L)R_{sx}$. In relation to the proposed OTA, the mobility reduction μ causes the transconductance parameter K that is μ dependent to change. This in turns causes variation in g_m or I_{out}. Thus, the g_m' can be further modified as $g'_m = 2K/[1 + 2KR_{sx}(V_{GS} - V_{T0} - \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}))]$. In fact, the drain current in a MOS transistor increases slightly as a result of the extension of the depletion layer at the drain into the channel towards the source over a short distance.

Thus the channel length is reduced and it is called short channel effect. To characterize this effect, a channel length modulation parameter λ is introduced. The parameter determines the slope of the output characteristic (I_D versus V_{DS}) of a MOS device where V_{DS} is the drain-to-source voltage. The resultant drain current in saturation is thus given by,

$$I_D = K (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{3.10}$$

This resultant drain current as a result of the short channel effect will cause I_{out} to vary from its ideal expression as given in equation (3.4). Note that for short-channel lengths the λ parameter is larger than for long-channel lengths. Thus, λ is critical in deep-submicron. Although using large geometry process can reduce the short channel effects, other performances such as the parasitic effects, power consumption, and speed are degraded. Therefore, there is a trade-off between transistor sizes.

For voltage-mode MLF IFLF filter implementation, four input two output OTAs are needed. The four input two output OTA based on the basic structure in Figure 3.1 is generated by an additional input pair in parallel and is presented in Figure 3.3.

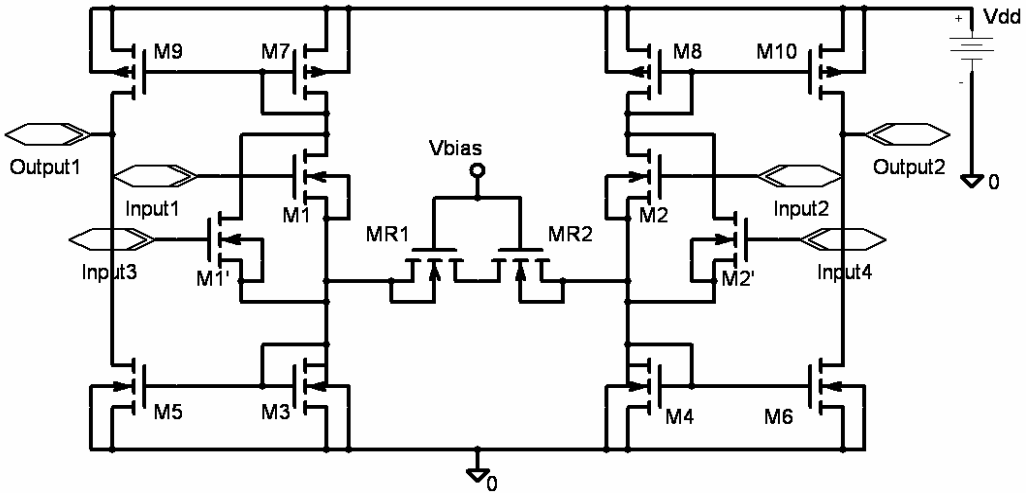


Figure 3.3 Fully-balanced four input two output OTA

3.2.3 Simulation Results of Transistor-level OTAs

Figures 3.4 and 3.5 show the hand calculated and simulated DC characteristics of the MO–OTA terminated by a short–circuit load and with 2V power supply voltage.

The transconductance turning range is from 800μS to 1.17mS, corresponding to values of I_1 from 1μA to 150μA.

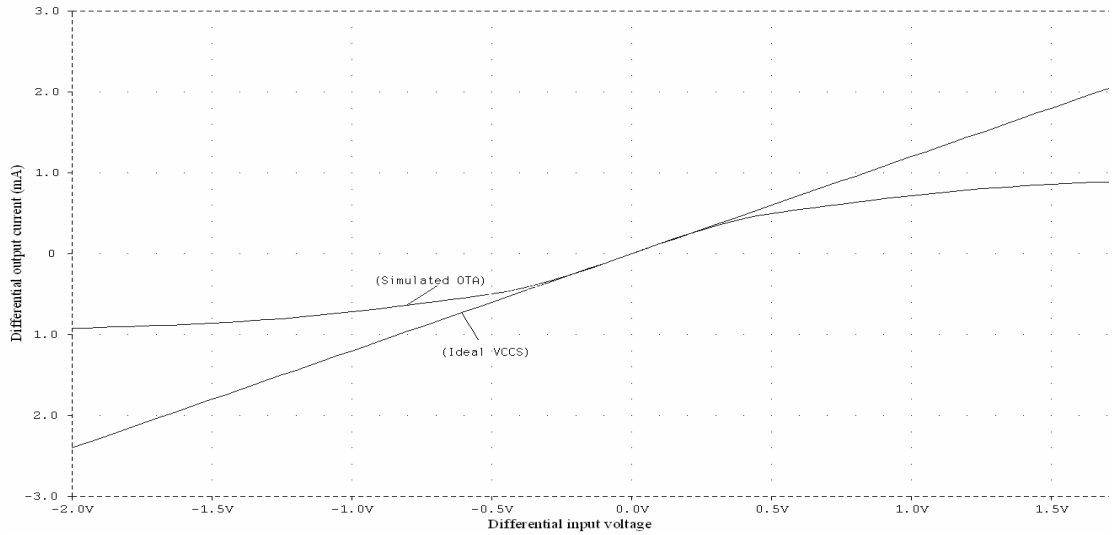


Figure 3.4 Simulated and hand calculated differential output current versus differential input voltage for the 2V OTA with short-circuit load

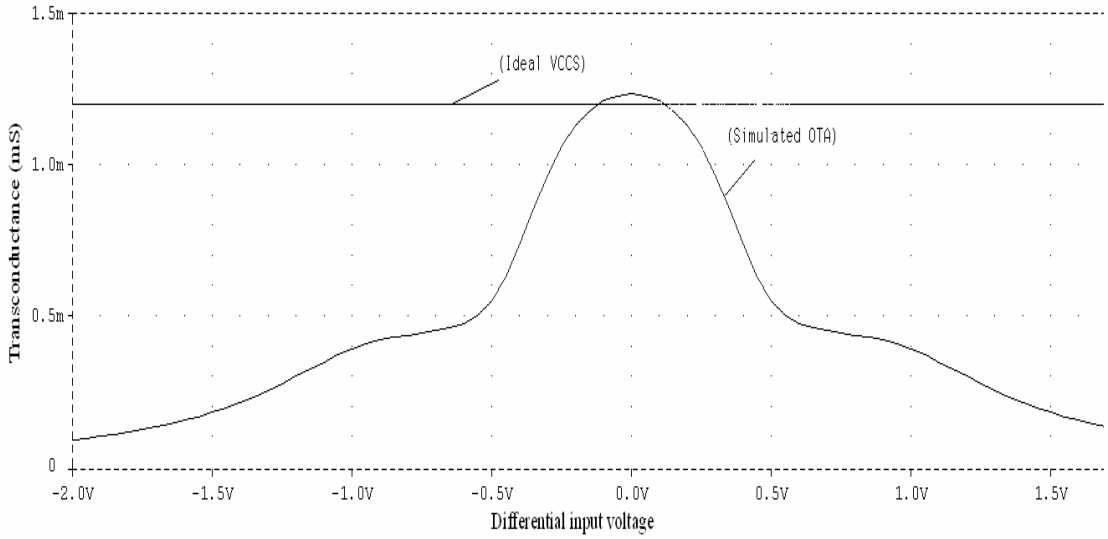


Figure 3.5 Simulated and hand calculated DC transconductance versus differential input voltage for the 2V OTA with short-circuit load

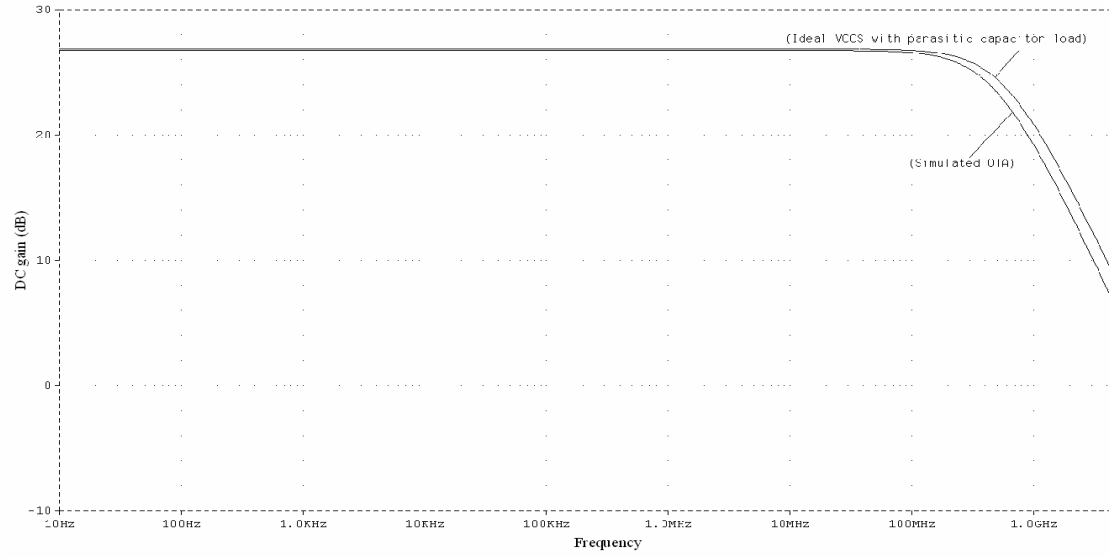


Figure 3.6 Simulated and hand calculated AC open-circuit frequency responses of the 2V OTA

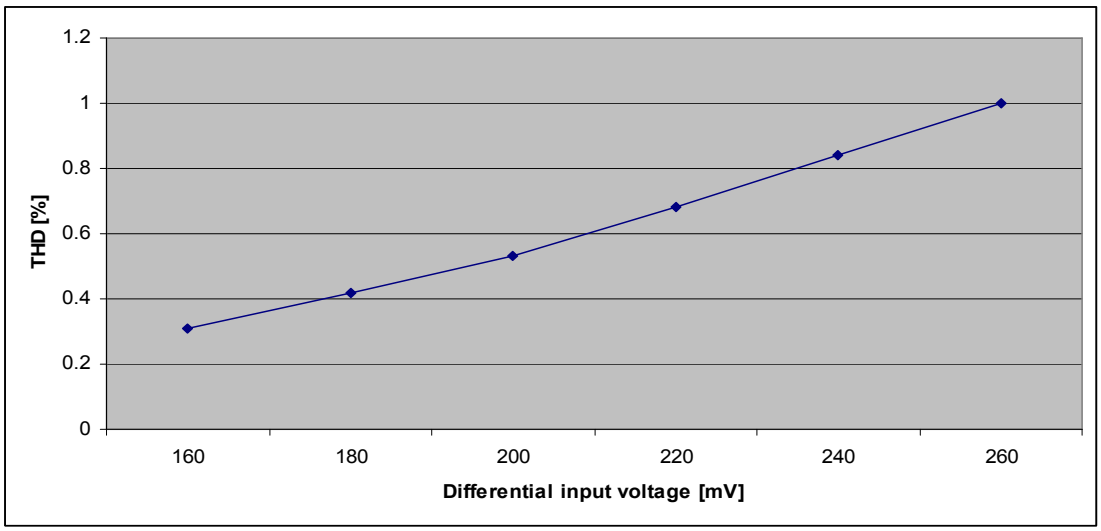


Figure 3.7 Simulated THD versus the differential input voltage of the 2V OTA

The THD of the presented OTA remains less than 1% at 260mV differential input voltage. Simulated and hand calculated results of OTA open–circuit responses are shown in Figure 3.6. The simulated open-circuit cut-off frequencies of the OTA cell are about 612MHz and 652MHz for the minimum and maximum bias current, respectively. The DC gain is around 27dB, which is adequate for low–Q applications.

Moreover, the higher cut-off frequency of the filter needs the larger OTA transconductance.

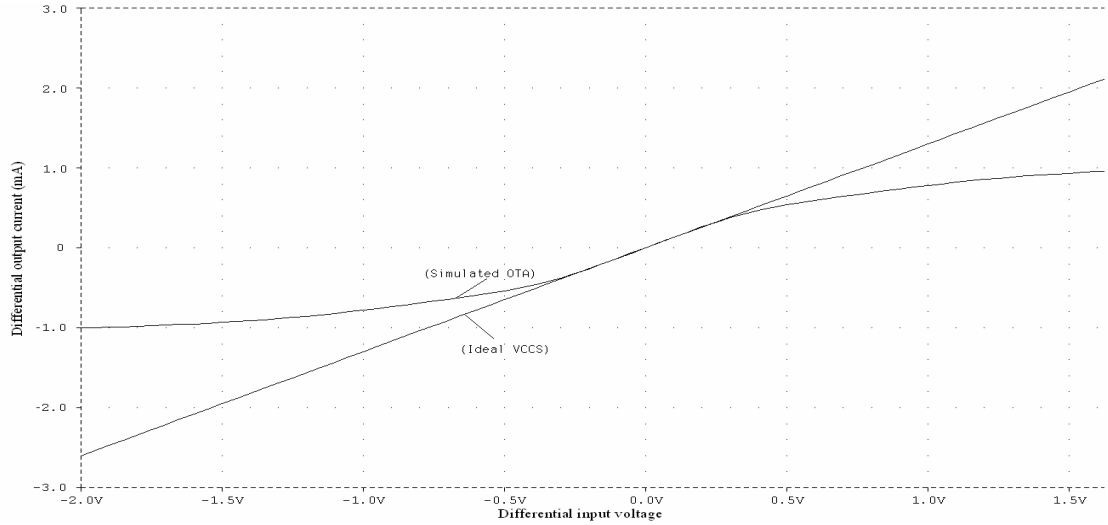


Figure 3.8 Simulated and hand calculated differential output current versus differential input voltage of the 2.5V OTA with short-circuit load

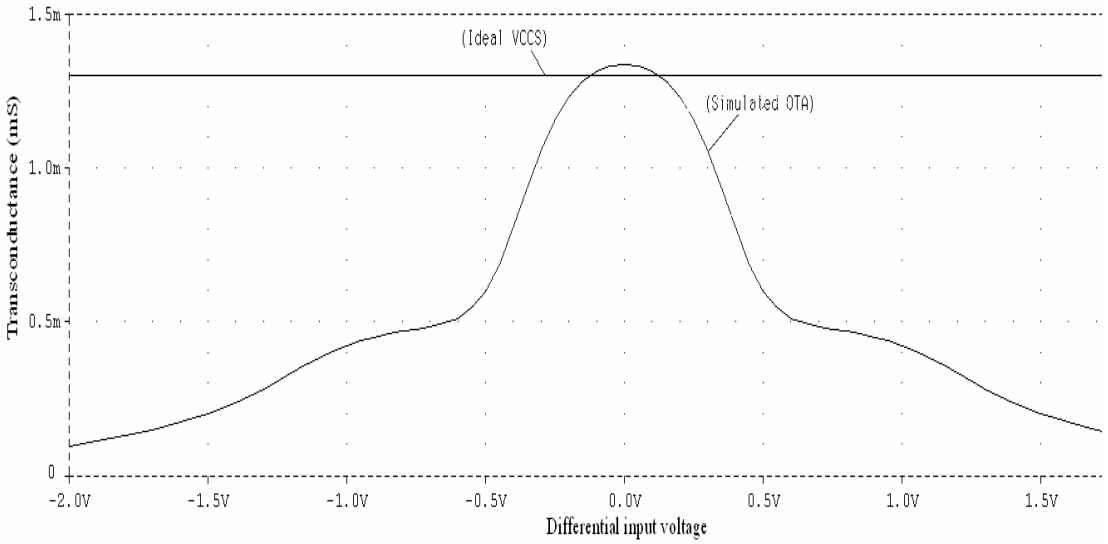


Figure 3.9 Simulated and hand calculated DC transconductance versus differential input voltage of the 2.5V OTA with short-circuit load

In order to further enhance the cut-off frequency of the proposed OTAs, the power supply voltage is reset up to 2.5V and the transconductance of OTA is redesigned as

1.3mS. The simulated DC responses of the modified OTA are shown in Figure 3.8 and 3.9, respectively.

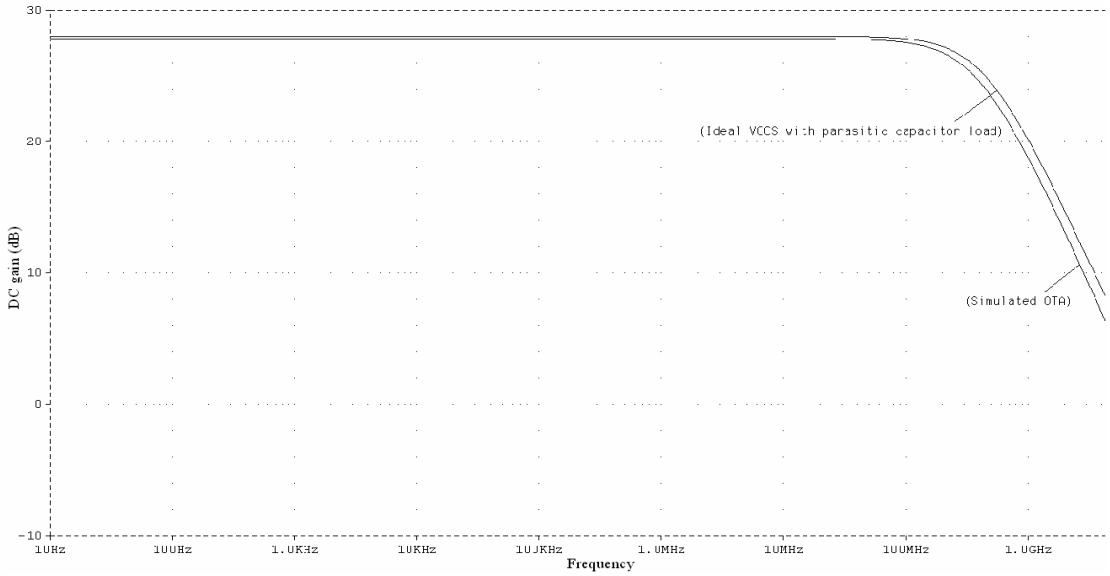


Figure 3.10 Simulated and hand calculated AC open-circuit frequency responses of the 2.5V OTA

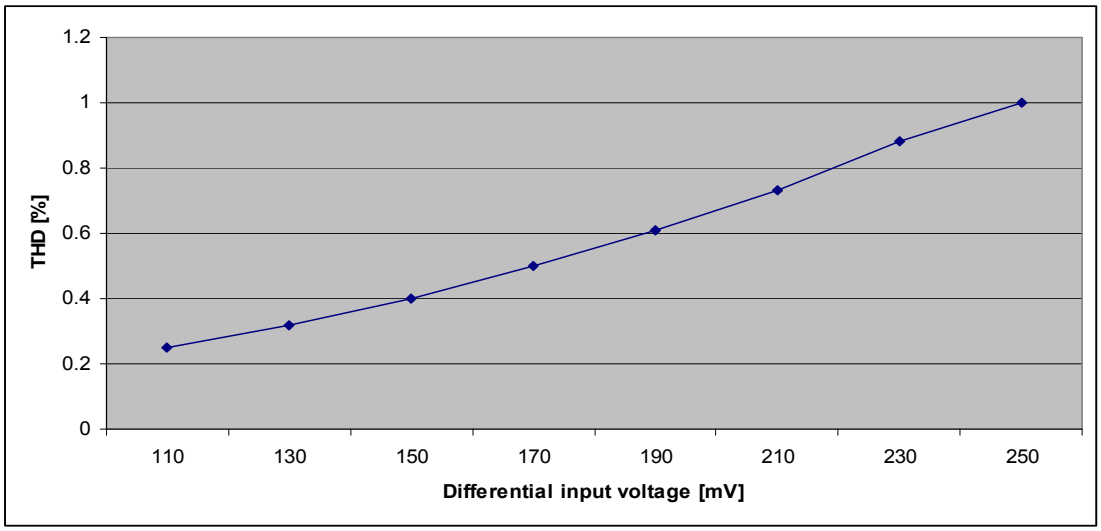


Figure 3.11 Simulated THD versus the differential input voltage of the OTA in Figure 3.3

The turning range of transconductance is from 935μS to 1.33mS, corresponding to values of I_1 from 1μA to 150μA. Simulated and hand calculated results of OTA open−circuit responses is shown in Figure 3.10. The simulated open-circuit cut-off

frequencies of the 2.5V OTA cell are about 635MHz and 597MHz for the minimum and maximum bias current, respectively. The THD of the presented OTA is less than 1% at 250mV differential input voltage.

3.3 Design of Current-mode 0.05° Equiripple Linear Phase MLF FLF OTA-C Lowpass Filters

Design of analogue integrated and signal processing circuits using the current-mode approach has been receiving considerable interest [1, 2, 4, 55-59, 104-108, 114]. This is because the approach offers higher performance (speed, bandwidth, accuracy, noise, and dynamic range), is more suitable for low-voltage and low-power operations, and reduces circuit structure complexity compared with its voltage-mode counterpart. Current-mode signal processing techniques have been widely used, in particular, in high frequency filtering applications. For example, mixed voltage and current equations are scaled into current-only ones in the design of active filters based on the simulation of passive LC ladders [105]. To realize a voltage transfer function, it is now preferred to cascade a current transfer function, a transadmittance function, and a transimpedance function section to benefit from the current-mode approach.

The OTA-C filter structures that have been dealt with in the literature are mainly based on voltage integrators and voltage amplifiers. They are useful for voltage signal processing with voltage inputs to OTA input terminals and voltage outputs from filter circuit nodes. For current-mode OTA-C filters, we can expect these filters are based on current integrators and current amplifiers. These circuits can perform current signal processing with current inputs to circuit nodes and current outputs from OTA output terminals. The structures of the basic current-mode building blocks: integrators and amplifiers can be understood from the current description point of view. For example, a current integrator has a capacitor connected to one of the input terminals of the OTA. The capacitor of the integrator converts the input current signal to a voltage signal and the OTA does the conversion from the voltage to the output current. For a current amplifier, an OTA resistor replaces the capacitor in the current integrator. Dual- and

multiple-output OTAs (DO-OTA and MO-OTA) that are suitable and used for current-mode signal processing and filtering applications have been reported [56-59, 104-108]. The study of the current-mode DO-OTA filters began in late 1970s, where current-mode filters based on one or two DO-OTAs were presented. Recently, many current-mode biquads and high-order filters based on DO-OTA or MO-OTAs have been reported. In particular, many new multiple loop feedback filter structures based on DO-OTA-C or MO-OTA-C integrators have been presented. These structures are useful for both canonical and non-canonical realizations of various filtering characteristics. The general all-pole and transmission zero structures presented in this section are single-ended. In practical filter designs, to achieve better common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), fully-balanced topology will be used.

3.3.1 Synthesis of Current-Mode FLF Lowpass OTA-C Filters

The current-mode n^{th}-order transfer function is given below:

$$H(s) = \frac{A_n s^n + \cdots + A_2 s^2 + A_1 s + A_0}{B_n s^n + \cdots + B_2 s^2 + B_1 s + 1} \tag{3.11}$$

The current-mode all-pole MLF FLF configuration is shown in Figure 3.10 below.

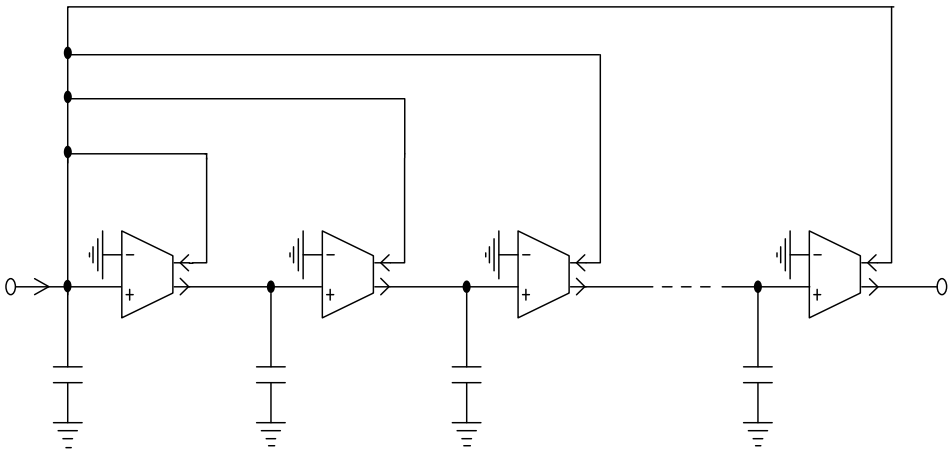


Figure 3.12 General all-pole current-mode MLF FLF OTA-C configuration

Writing the circuit current transfer function and comparing this function with

equation 3.11, where $\tau_j = c_j/g_j$. We can establish the following equations [119, 123]:

$$\tau_n = B_{1,}\tau_j = \frac{B_{n-j+1}}{B_{n-j}} \qquad (j = n-1, n-2, ..., 1) \tag{3.12}$$

The current-mode single-ended n^{th}-order MLF FLF configuration with input distribution structure is shown in Figure 3.13. As can be seen from Figure 3.12, the input, output and feedback signals all are current signals. The structure consists of a current amplifiers and current integrators. The input current is firstly converted by the grounded OTA g_r into voltage.

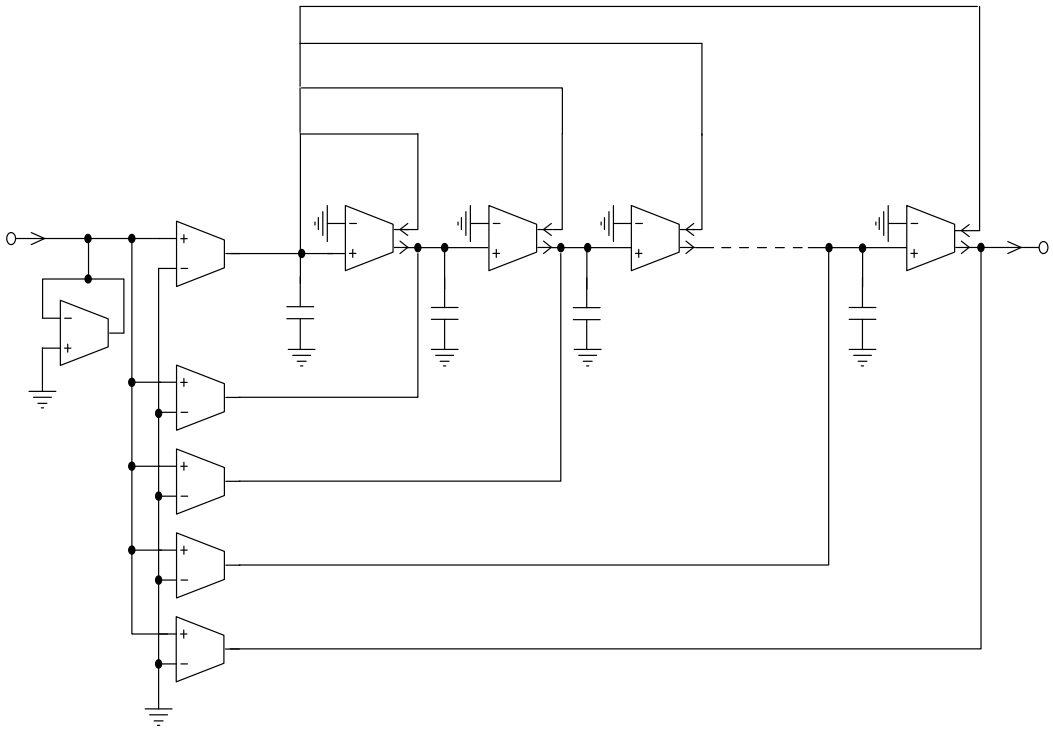


Figure 3.13 The single-ended current-mode MLF FLF structure with input distribution

Writing the circuit current transfer function and comparing this function with equation 3.11, where $\beta_j = g_{aj}/g_j$. We can establish the following equations:

$$\beta_0 = \frac{A_n}{B_n}, \beta_1 = A_0 - \beta_0 - \sum_{i=0}^{n-2} \beta_{n-i},$$
$$\beta_j = \frac{B_{n-j+1}}{B_n}[A_{j-1} - \beta_0 B_{j-1} - \sum_{i=0}^{n-j-1} \beta_{n-i} \frac{B_{j+i}}{B_{1+i}}], \ (j = n-1, n-2, ..., 2) \quad (3.13)$$
$$\beta_n = \frac{B_1(A_{n-1} - \beta_0 B_{n-1})}{B_n}$$

The current-mode single-ended n[th]-order MLF FLF configuration with output summation structure is shown in Figure 3.14.

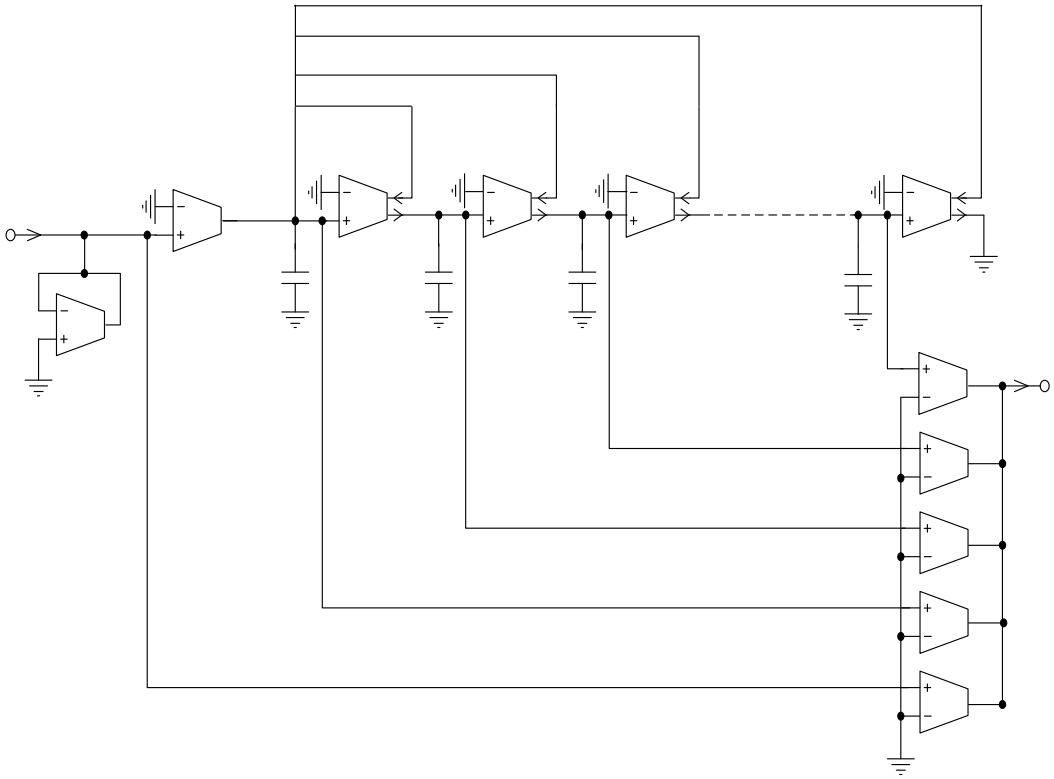


Figure 3.14 The single-ended current-mode MLF FLF structure with output summation

Writing the circuit current transfer function in Figure 3.14 above and comparing this function with equation 3.11, Where $\alpha_j = g_{aj}/g_j$, we can derive the following equations:

$$\alpha_0 = \frac{A_n}{B_n}, \alpha_j = \frac{A_{n-j}}{B_{n-j}} - \alpha_0, \alpha_n = A_0 - \alpha_0$$

$$(j = n-1, n-2, ..., 2) \tag{3.14}$$

3.3.2 Design of Seventh-order Current-mode FLF 0.05° Equiripple Linear Phase Lowpass OTA-C Filter

The normalized characteristic of a seventh-order 0.05° equiripple linear phase lowpass filter with real zeros at the cut-off frequency is given by:

$$H_d(s) = \frac{s^2 - 1}{D(s)} \tag{3.15}$$

with

$$D(s) = 0.05561\, s^7 + 0.291094\, s^6 + 1.095656\, s^5 + 2.554179\, s^4 + 4.255922\, s^3 + 4.676709\, s^2 + 3.176156\, s + 1$$

The fully balanced realization of the function in equation 3.15 using the current–mode MLF FLF structure with output summation OTAs is shown in Figure 3.15.

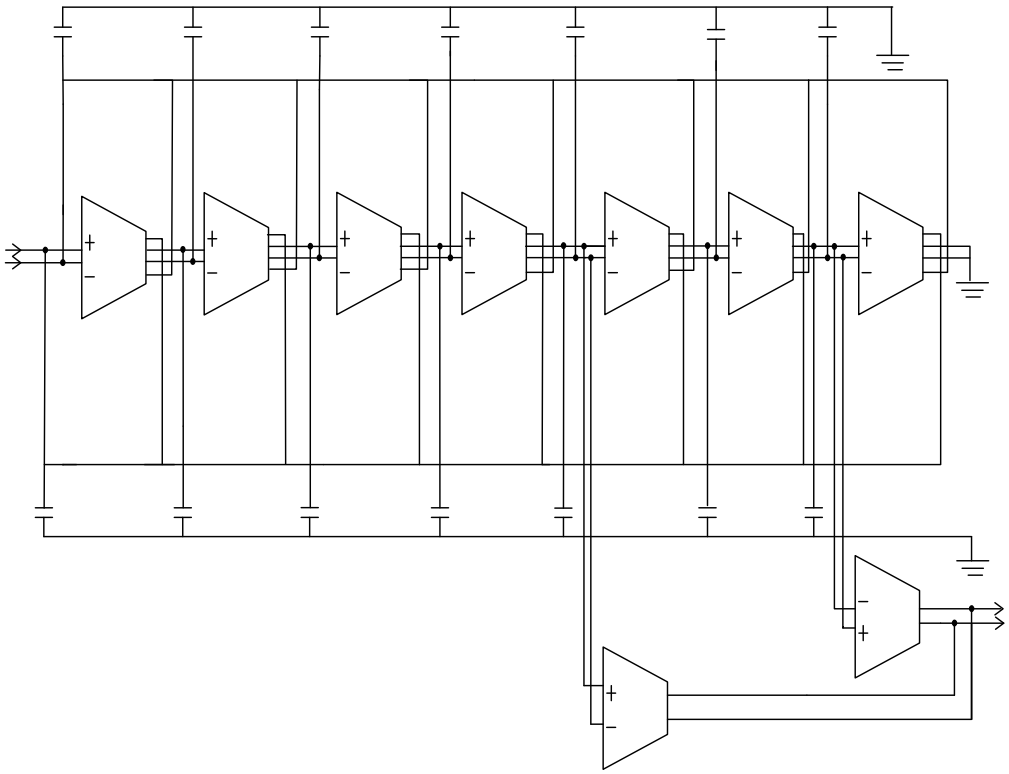


Figure 3.15 Seventh–order current–mode FLF OTA–C lowpass filter with output summation OTA network

The overall transfer function of the circuit can be derived as

$$H(s) = \frac{I_{output}}{I_{input}} = \frac{N(s)}{D(s)} \tag{3.16}$$

where

$$N(s) = \alpha_5 \tau_6 \tau_7 s^2 + \alpha_7$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^6 + \tau_3\tau_4\tau_5\tau_6\tau_7 s^5 + \tau_4\tau_5\tau_6\tau_7 s^4 + \tau_5\tau_6\tau_7 s^3 + \tau_6\tau_7 s^2 + \tau_7 s + 1$$

where $\tau_j = c_j/g_j$, $\alpha_j = g_{aj}/g_j$. The design formulae for the lowpass filter can be attained by coefficient matching between equations (3.15) and (3.16) [106, 107].

$$\tau_1 = \frac{B_7}{B_6}, \tau_2 = \frac{B_6}{B_5}, \tau_3 = \frac{B_5}{B_4}, \tau_4 = \frac{B_4}{B_3}, \tau_5 = \frac{B_3}{B_2}, \tau_6 = \frac{B_2}{B_1},$$

$$\tau_7 = B_1, \alpha_5 = \frac{A_2}{B_2}, \alpha_7 = A_0$$

The resulting pole and zero parameters can be calculated as:

$$\tau_1 = 0.19106\ , \tau_2 = 0.26568\ , \tau_3 = 0.42897\ , \tau_4 = 0.60015\ , \tau_5 = 0.91002\ ,$$
$$\tau_6 = 1.47244\ , \tau_7 = 3.17616\ , \alpha_5 = 0.213826\ , \alpha_7 = 1$$

(3.17)

The filter is designed with identical transconductances g_j (j = 1 to 7) using the CMOS OTA cell in Figure 3.2, with selected transconductance of 800μS, to improve OTA matching and facilitate design automation. The cut–off frequency of the filter is chosen as 150 MHz. Using the computed parameter values in equation (3.17), the capacitance and transconductance values can be calculated as:

$$C_1 = 0.3244pF, C_2 = 0.451pF, C_3 = 0.7282pF, C_4 = 1.0188pF, C_5 = 1.5449pF,$$
$$C_6 = 2.5pF, C_7 = 5.392pF, g_{a5} = 170\mu S, g_{a7} = 800\mu S$$

However, the parasitic capacitance must be taken into account. For the circuit of Figure 3.2, the parasitic capacitance is about $0.1pF$. Thus, the grounded capacitor values can be recalculated as:

$$C_1 = 0.2244pF, C_2 = 0.351pF, C_3 = 0.6282pF, C_4 = 0.9188pF, C_5 = 1.4449pF,$$
$$C_6 = 2.4pF, C_7 = 5.292pF$$

3.3.3 Design of Fifth-order Current-mode FLF 0.05° Equiripple Linear Phase Lowpass OTA-C Filter

The normalized characteristic of a fifth−order 0.05° equiripple linear phase lowpass filter with real zeros (gain boost) is given by:

$$H_d(s) = \frac{(s^2 - 1)}{D(s)} \tag{3.18}$$

with

$$D(s) = 0.201926\, s^5 + 0.822285\, s^4 + 2.075924\, s^3 + 3.033116\, s^2 + 2.604527\, s + 1$$

The fifth-order FLF filter configuration is shown in Figure 3.16 to realize the transfer function.

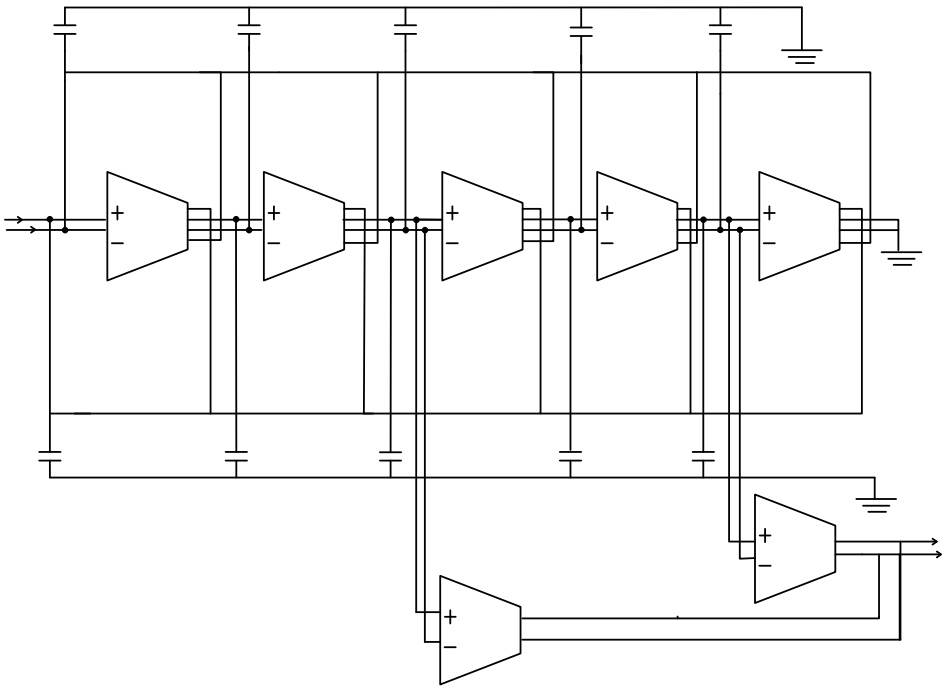


Figure 3.16 Fifth-order current-mode FLF OTA-C filter with output summation OTA network

The overall transfer function of the circuit can be derived as:

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{N(s)}{D(s)} \tag{3.19}$$

where

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + \tau_3\tau_4\tau_5 s^3 + \tau_4\tau_5 s^2 + \tau_5 s + 1$$
$$N(s) = \alpha_3\tau_4\tau_5 + \alpha_5$$

where $\tau_j = c_j/g_j$, $\alpha_j = g_{aj}/g_j$. The design formulae for the filter can be attained by coefficient matching between equations 3.18 and 3.19. The resulting pole and zero parameters are:

$$\tau_1 = 0.2456\ ,\tau_2 = 0.3961\ ,\tau_3 = 0.6844\ ,\tau_4 = 1.1646\ ,\tau_5 = 2.6045\ ,$$
$$\alpha_3 = 0.213826\ ,\alpha_5 = 1$$

The filter is designed with identical unit OTAs using the CMOS OTA cell in Figure 3.2, with 2.5V power supply voltage and selected transconductance of 1.2mS. The cut-off frequency of the filter is chosen as 300 MHz. Using the computed parameter values and taking into account the parasitic capacitance, the capacitance and transconductance values can be calculated as:

$$C_1 = 0.2127\ \ pF\ ,\ C_2 = 0.4043\ \ pF\ ,\ C_3 = 0.7714\ \ pF\ ,$$
$$C_4 = 1.3828\ \ pF\ ,\ C_5 = 3.2162\ \ pF\ ,$$
$$g_{a3} = 260\ \mu S\ ,\ g_{a5} = 1.2\,mS$$

3.4 Design of Voltage-mode Seventh-order IFLF 0.05° Equiripple Linear Phase Lowpass OTA-C Filter

The voltage-mode IFLF MLF configuration has not been widely used for HDD systems in the literature. The highest speed achieved so far using the IFLF filter for read channels is about 20MHz, which is far below the speed of current-mode MLF FLF filters. In this section, we design a voltage-mode seventh-order IFLF 0.05° equiripple linear phase OTA-C lowpass filter to achieve a very high frequency using 0.18μm CMOS technology. The normalized characteristic of a seventh-order 0.05° equiripple linear phase lowpass filter with real zeros is already given in equation 3.15. The fully balanced realization of the function in equation 3.15 using the voltage-mode MLF IFLF structure with input distribution OTAs is shown in Figure 3.17.

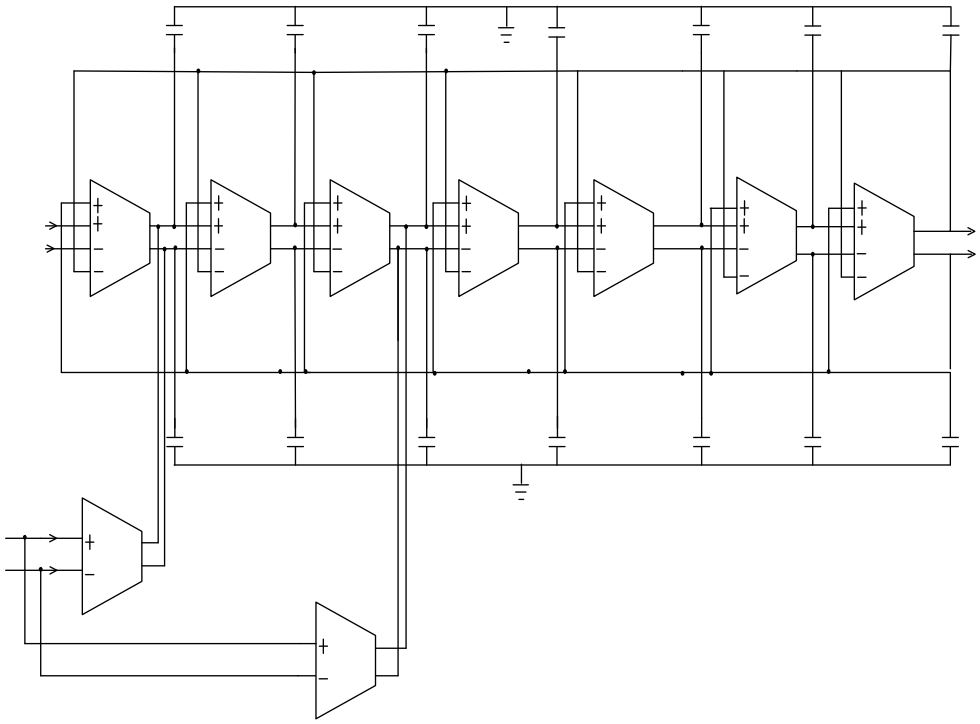


Figure 3.17 Voltage-mode seventh-order IFLF OTA–C filter with input distribution OTA network

The overall transfer function of the circuit can be derived as:

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{N(s)}{D(s)} \qquad (3.20)$$

Where

$$N(s) = \beta_3 \tau_1 \tau_2 s^2 + \beta_1$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 + \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 + \tau_1 s + 1$$

where $\tau_j = c_j/g_j$, $\beta_j = g_{aj}/g_j$. The design formulae for the filter can be attained by coefficient matching between equations (3.15) and (3.20), given by:

$$\tau_1 = B_1, \tau_2 = \frac{B_2}{B_1}, \tau_3 = \frac{B_3}{B_2}, \tau_4 = \frac{B_4}{B_3}, \tau_5 = \frac{B_5}{B_4}, \tau_6 = \frac{B_6}{B_5}, \tau_7 = \frac{B_7}{B_6}$$

$$\beta_3 = \frac{A_2}{B_2}, \beta_1 = A_0$$

The resulting pole and zero parameters are:

$$\tau_7 = 0.19106\ ,\ \tau_6 = 0.26568\ ,\ \tau_5 = 0.42897\ ,\ \tau_4 = 0.60015\ ,\ \tau_3 = 0.91002\ ,$$
$$\tau_2 = 1.47244\ ,\ \tau_1 = 3.17616\ ,\ \beta_1 = 0.213826\ ,\ \beta_3 = 1$$

(3.21)

The filter is designed with identical unit OTAs g_j (j =1 to 7) using the CMOS OTA cell in Figure 3.3, with selected transconductance of 1.2mS. The cut-off frequency of the filter is chosen as 400 MHz. Using the computed parameter values in equation (3.21), the capacitance and transconductance values are obtained as:

$$C_7 = 0.0824\ pF\ ,\ C_6 = 0.1537\ pF\ ,\ C_5 = 0.3096\ pF\ ,\ C_4 = 0.4731\ pF\ ,$$
$$C_3 = 0.769\ pF\ ,\ C_2 = 1.3061\ pF\ ,\ C_1 = 2.933\ pF\ ,$$
$$g_{a1} = 260\ \mu S,\ g_{a3} = 1.2\,mS$$

3.5 Simulation Results of Current-mode FLF and Voltage-mode IFLF OTA-C Filters

3.5.1 Simulation Results of Current-mode Seventh-order 0.05° equiripple linear phase FLF lowpass OTA-C filter

The filter circuit in Figure 3.15 was simulated using the component which designed in section 3.3.2 and OTA in Figure 3.2, using BSIM 3v3 Spice models for a TSMC 0.18μm CMOS process available from MOSIS [112, 113]. Figure 3.18 shows the magnitude response of the current-mode seventh-order 0.05° equiripple linear phase lowpass filter with and without the gain boost with 2V power supply. As can be seen from Figure 3.18, the gain boost of the filter is about 5dB. By varying the bias current I_1 of the unit OTA cell, the tuning range of cut–off frequency without gain boost is 55−160MHz.

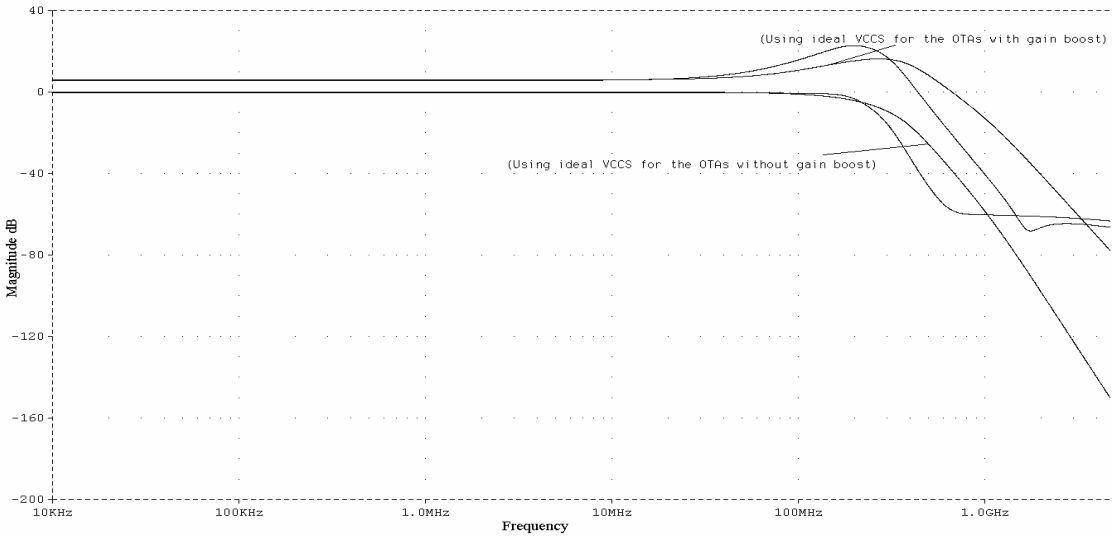


Figure 3.18 Simulated magnitude response of the current-mode FLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter without and with gain boost

As can be seen from Figure 3.18, although there is an unwanted zero for the proposed filter due to the hard-to-control phase errors, the cut-off frequency still matches our target specification.

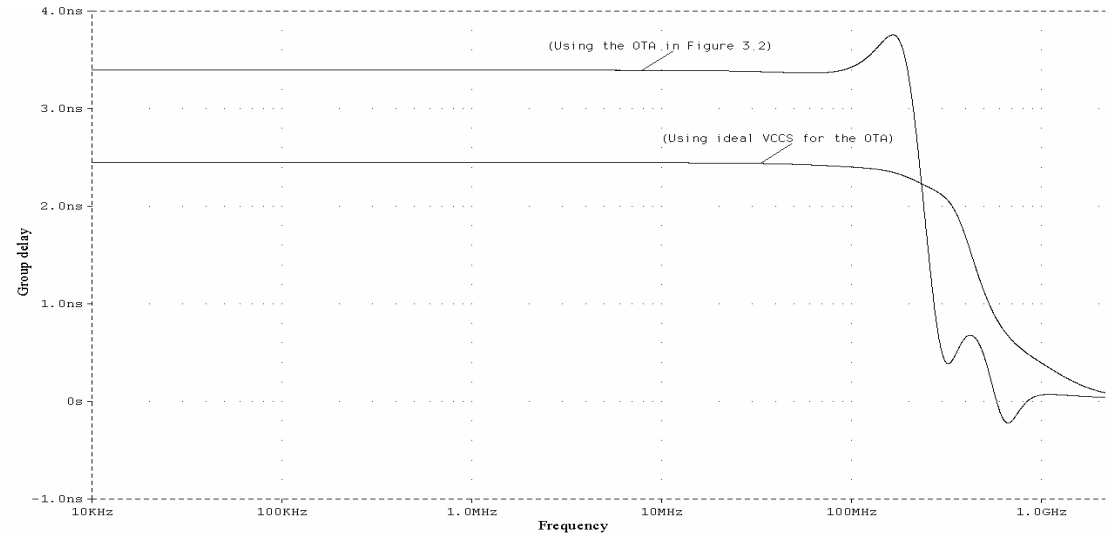


Figure 3.19 Simulated group delay response of the current-mode FLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

The filter phase response without gain boost is fairly linear, as can be seen from Figure 3.19. The group delay has very small variation up to the cut–off frequency and

it is shown that the gain boost has minimal effect on the group delay ripple of the filter, with two real zeros added into the filter response. The filter's group delay ripple for $0 \leq f \leq f_c$ is approximately 4% with the group delay below ±250ps over the whole tuning range. This is well within the limit of the read channel filter specification. The simulated THD versus the differential input current of the proposed filter is shown in Figure 3.20. The dynamic range of the filter, defined as the RMS of the output current signal at 1% THD divided by the total RMS output noise current integrated over 160MHz, which is 240nA$_{RMS}$, is 45dB. The maximum power consumption of the proposed filter is only 15mW at 160MHz cut-off frequency.

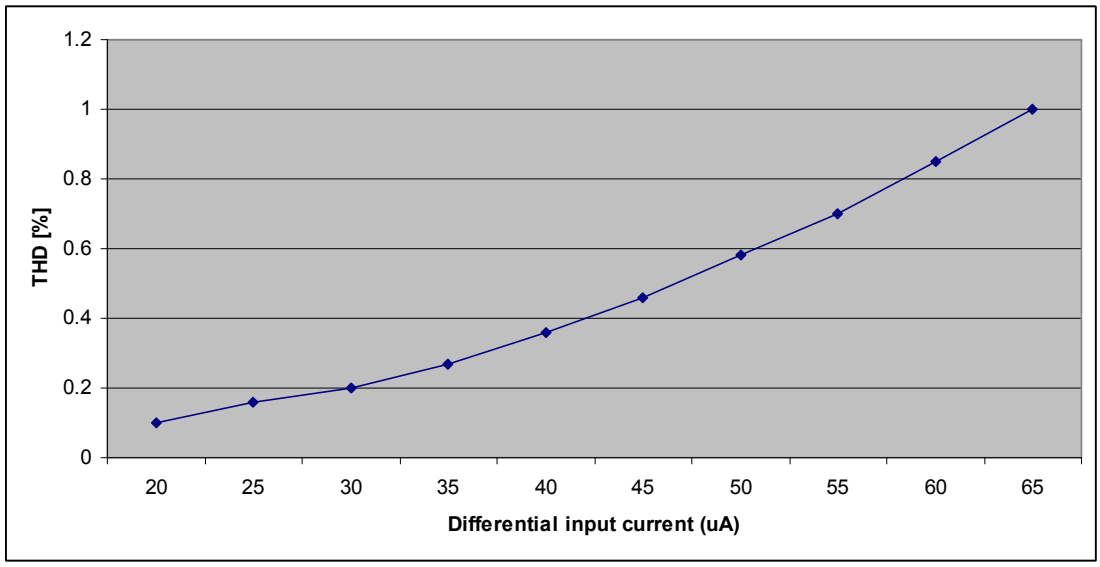


Figure 3.20 Simulated THD versus the differential input current of the current-mode FLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

It is shown in Figure 3.20 that 1% THD of the proposed filter in Figure 3.5 can be achieved for the differential input current up to 65uA. The THD versus frequency is also simulated and shown in Figure 3.21. As can be seen, the THD remains less than 1% up to 135MHz.

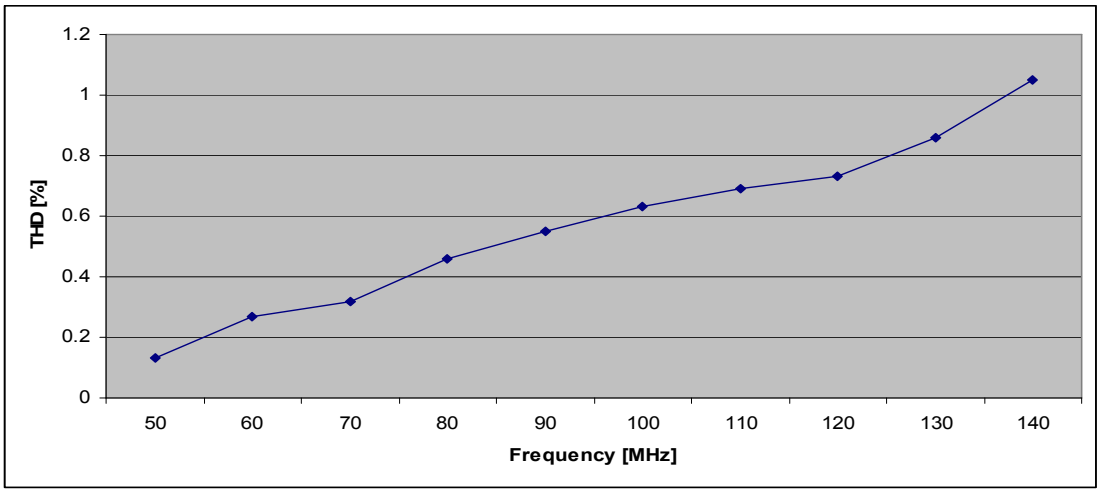


Figure 3.21 Simulated THD versus the frequency of the current-mode FLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

3.5.2 Simulation Results of Current-mode Fifth-order 0.05° Equiripple Linear Phase FLF OTA-C Lowpass Filter

Using the OTA in Figure 3.2 with 2.5V supply voltage and computed values obtained in section 3.3.3, the simulated magnitude and group delay ripple responses of the fifth-order current-mode 0.05° equiripple linear phase lowpass FLF filter in Figure 3.16 are simulated in 0.18µm CMOS and are shown in Figure 3.22 and 3.23, respectively.

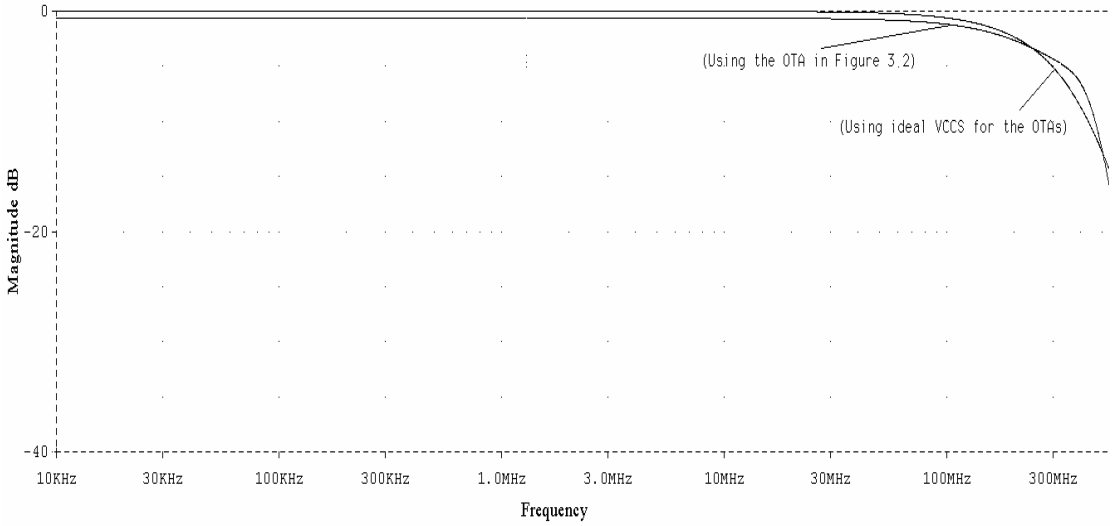


Figure 3.22 Simulated magnitude response of the current-mode FLF fifth-order 0.05° equiripple linear phase OTA-C lowpass filter

As can be seen from Figure 3.22 and 3.23, although the parasitic capacitance has been extracted from the grounded capacitors, there are still some deviation between ideal and practical simulation results.

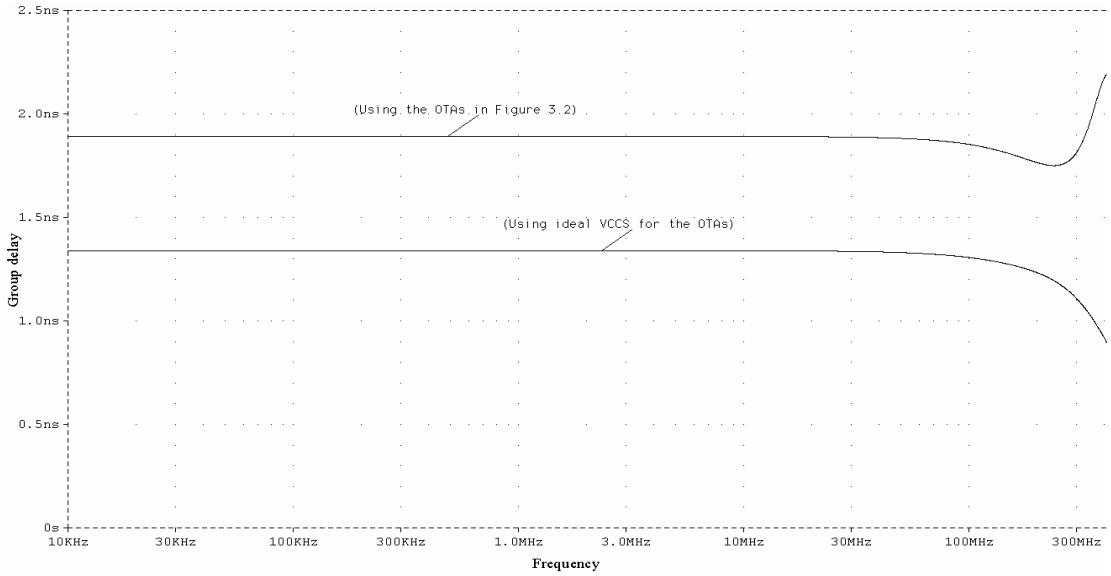


Figure 3.23 Simulated group delay ripple of the current-mode fifth-order 0.05° equiripple linear phase FLF OTA-C lowpass filter without gain boost

The group delay ripple is relatively higher than its seventh-order counterpart, which has been proved in chapter 2. The filter group delay ripple up to twice the cut-off frequency is approximately 12%, which is higher than the read channel filter specification (≤5%). Figure 3.24 shows THD versus the differential input current of the proposed fifth-order filter. Less than 1% THD has been achieved at 500uA differential input current. Also, the THD versus frequency has been simulated in Figure 3.25. It is shown from Figure 3.25; the THD of the proposed filter in Figure 3.6 is less than 1% for the frequency up to 290MHz.

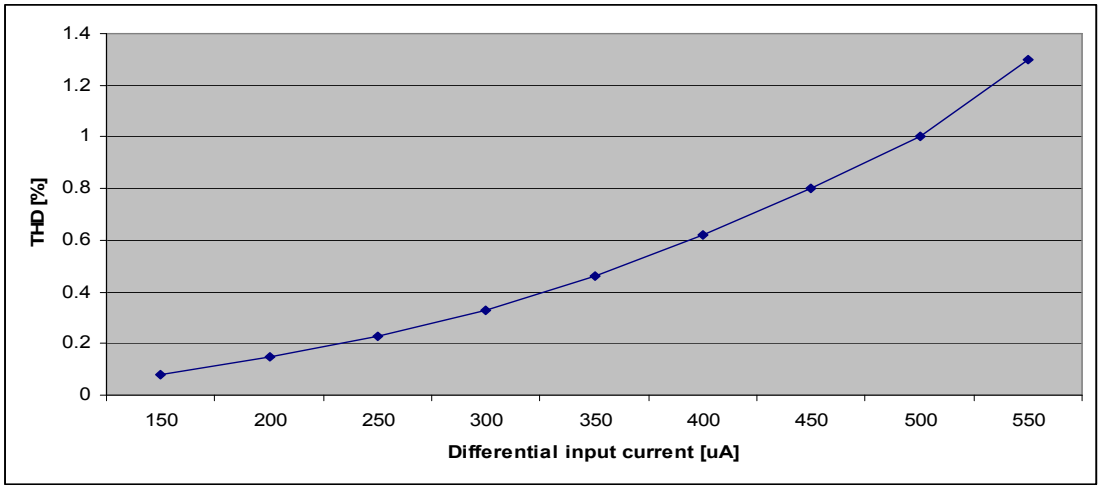


Figure 3.24 Simulated THD versus the differential input current of the current-mode FLF fifth-order 0.05° equiripple linear phase OTA-C lowpass filter

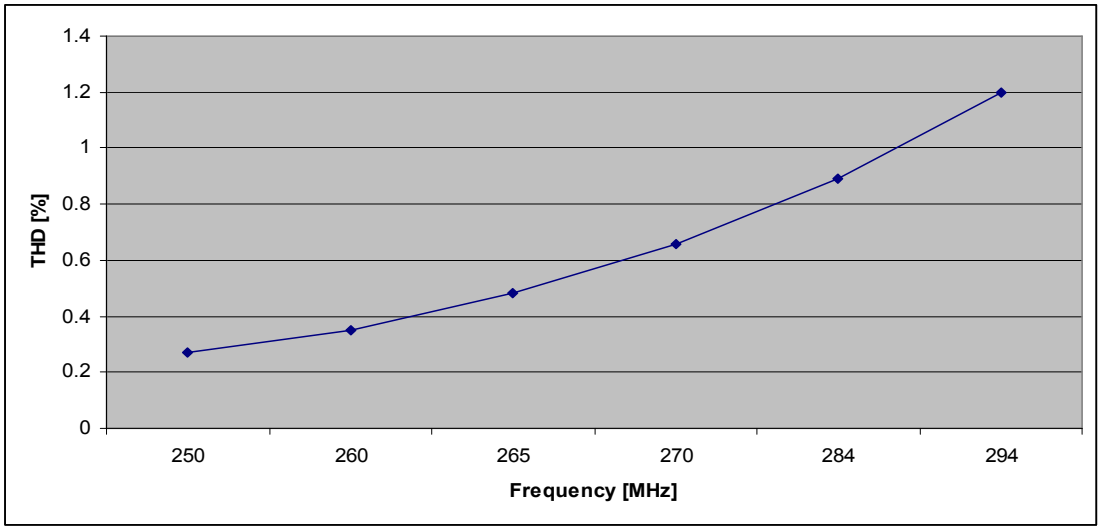


Figure 3.25 Simulated THD versus frequency of the current-mode FLF fifth-order 0.05° equiripple linear phase OTA-C lowpass filter

As is expected, the cut-off frequency of the fifth-order filter can be tuned up to 350MHz; the gain boost is around 8dB. Pspice simulation also shows that the power consumption of the filter is about 53mW at cut-off frequency of 300MHz. Using the same definition from the section 3.5.2, the THD is less than 1% with a single tone of 400μA at 300MHz and dynamic range of 54dB is obtained at *fc* =300MHz.

3.5.3 Simulation Results of Voltage-mode Seventh-order 0.05° Equiripple Linear Phase IFLF OTA-C Lowpass Filter

Using the OTA in Figure 3.3 with power supply voltage of 2.5V, ideal VCCS and component values calculated in section 3.4, the voltage-mode seventh-order 0.05° equiripple linear phase IFLF lowpass filter in Figure 3.17 is also simulated. As can be seen from Figure 3.26, there is only a small deviation in the magnitude frequency response between the results using the ideal VCCS and OTA in Figure 3.3 with power supply voltage of 2.5V, which is duo to parasitic effects. The cut-off frequency of the seventh-order filter is tunable from 290–430MHz. The total power consumption of the filter is about 78.7mW at 400MHz cut–off frequency for a single 2.5V power supply; the gain boost is around 8dB.

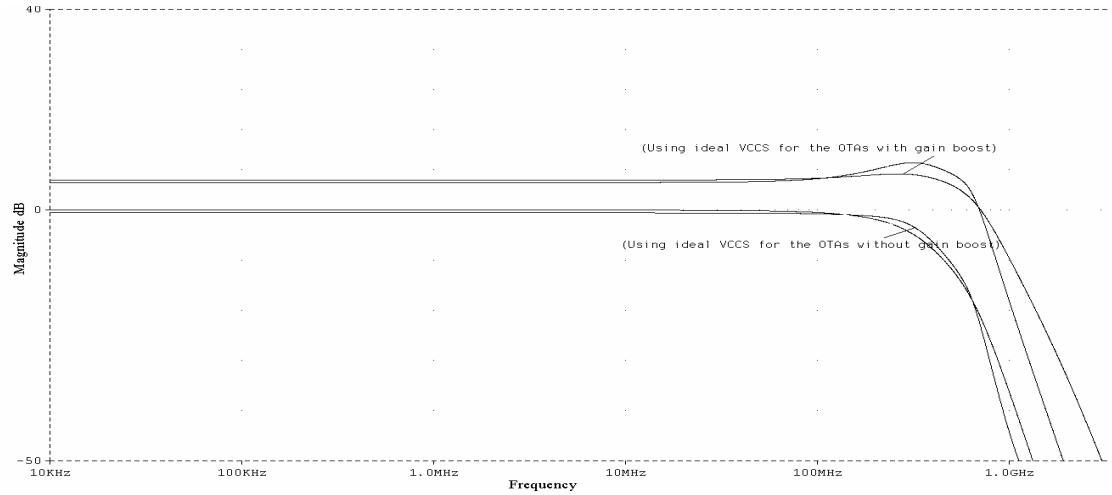


Figure 3.26 Simulated magnitude responses of the voltage-mode IFLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter without and with gain boost

The filter phase response is fairly linear, as shown in Figure 3.27. The filter group delay ripple up to cut-off frequency is approximately 6% (±100ps), which is slightly higher than the minimum read channel filter specification (≤5%). Simulations of the filter have also shown a total harmonic distortion (THD) of less than 1% with a single tone of 220μA at 400MHz. The dynamic range is about 52dB at the cut-off frequency of 400MHz. The noise spectrum is about 17.5nV$_{RMS}$/√Hz. Approximating integration

of noise over a bandwidth of 400MHz of the densities is about 550nV$_{RMS}$.

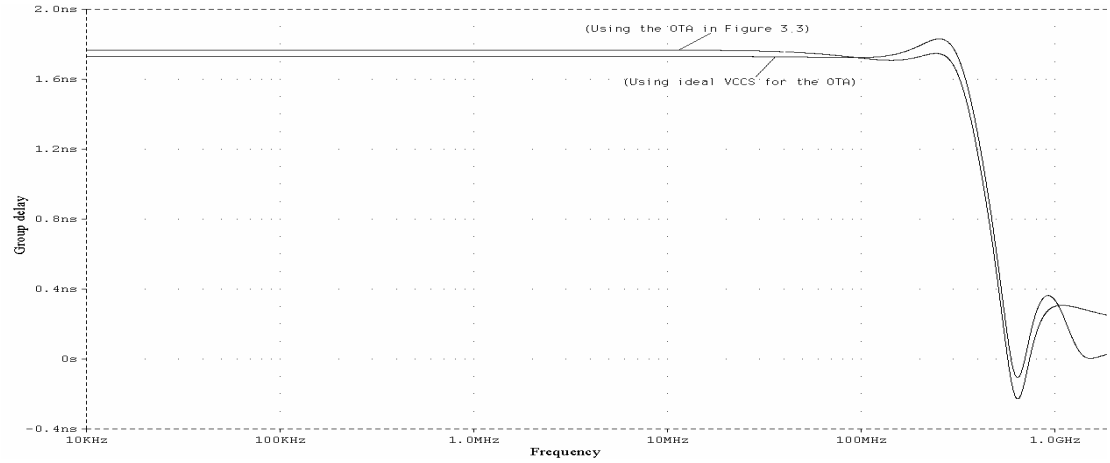


Figure 3.27 Simulated group delay responses of the voltage-mode IFLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter with and without gain boost

The THD of the proposed voltage-mode filter versus differential input voltage and frequency are also simulated, which are shown in Figures 3.28 and 3.29, respectively. As can be seen from Figure 3.28, the simulated THD is less than 1% for the differential input voltage up to 485mV. The simulation result in Figure 3.29 also shows that the THD is less than 1% at frequency up to 325MHZ.

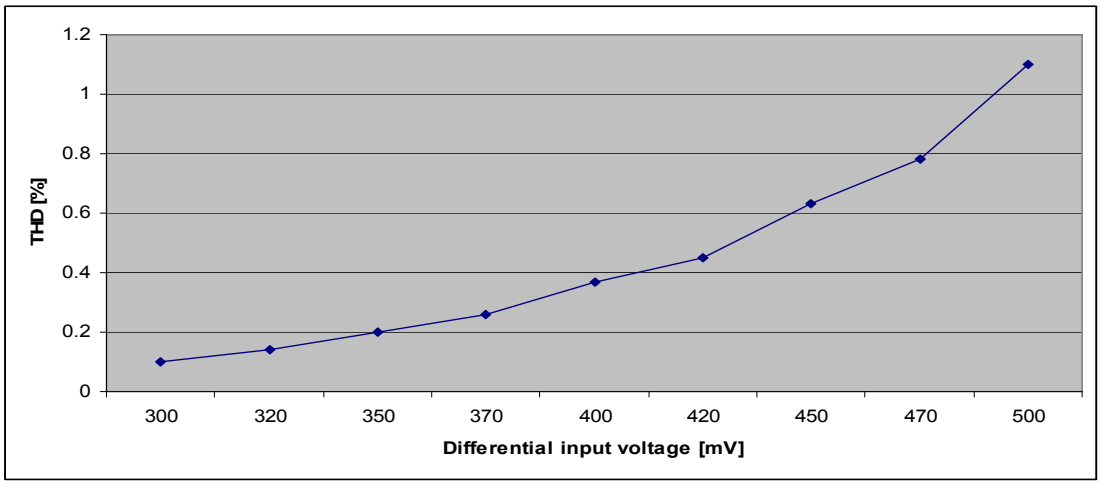


Figure 3.28 Simulated THD versus the differential input voltage of the voltage-mode IFLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

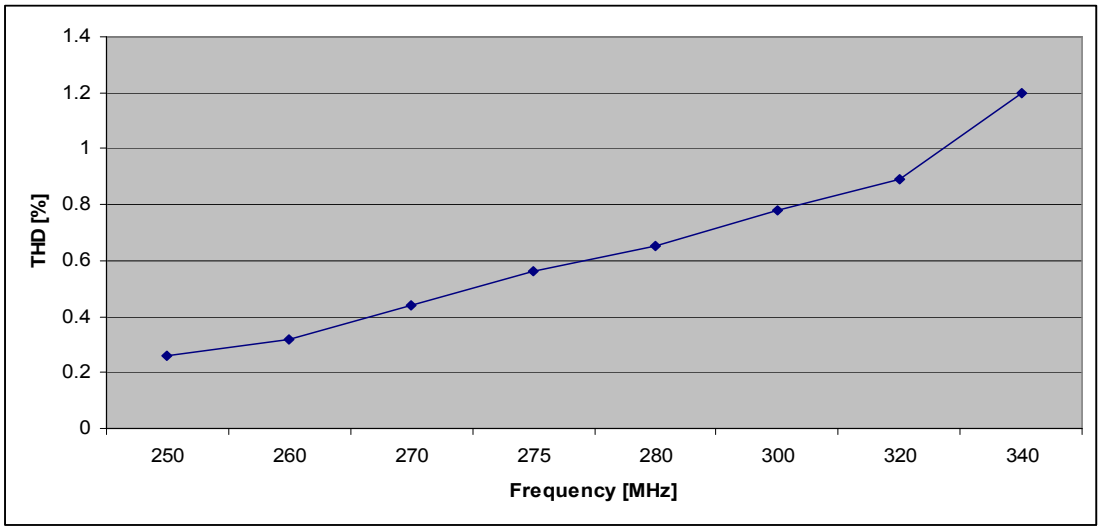


Figure 3.29 Simulated THD versus frequency of the voltage-mode IFLF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

A comparison of the simulated voltage-mode IFLF filters with target specifications is presented in Table 3.3 below. A comparison of the linear phase voltage-mode IFLF and current-mode filter designed and simulated in this chapter with other publication in the literature is also presented in Table 3.4.

Table 3.3 The Comparison of the simulated filter with target specifications

Specification	DR	PC	*fc*	GB	GDR
Target	35dB	100mW	300MHz	10dB	5%
Simulation	54dB	79mW	290-400MHz	8dB	6%

Table 3.4 Comparison with other seventh-order linear phase OTA-C filter designs

Filter type	Filter configuration	Process	*fc* range	GB	DR	FOM	GDR
VM IFLF (This work)	7^{th} order 0.05° equiripple linear phase	TSMC 0.18µm	290-430MHz	8dB	54dB	3927	6% up to *fc*
CM FLF [59]	7^{th} order 0.05° equiripple	TSMC 0.18µm	55-160MHz	9dB	45dB	2761	5% up to *fc*

(This work)	linear phase						
VM IFLF [42]	7th order 0.05° equiripple linear phase	MOSIS 2μm	5-20MHz	9dB	?	71	2.5% up to 2*fc*
VM LF [36]	7th order 0.05° equiripple linear phase	TSMC 0.25μm	8-32MHz	3dB	55dB	8.5	7% up to 1.1*fc*
VM LF [37]	7th order 0.05° equiripple linear phase	TSMC 0.25μm	50-150MHz	6dB	65dB	272	5% up to 1.5*fc*
CM LF [56]	7th order 0.05° equiripple linear phase	TSMC 0.18μm	260-320MHz	5dB	66dB	810	4.5% up to 1.5*fc*

Notes: f_c –cut-off frequency, GB – gain boost, VM – voltage-mode, CM – current-mode, DR – dynamic range, PS/PC – power supply/power consumption, GD – group delay, N/A - not applicable.

3.6 Conclusions

Fully-differential current-mode FLF and voltage-mode IFLF OTA-C filters have been studied in this chapter. The synthesis and performances of current-mode fifth- and seventh-order FLF and voltage-mode seventh-order IFLF 0.05° equiripple OTA-C lowpass filters are described. The filter structures are canonical and do not have any node that is without any capacitor to ground. All-pole filters are realized using the basic FLF and IFLF structures and filters with arbitrary transmission zeros are realized using output summation and input distribution OTA networks for current-mode and voltage-mode structures, respectively. To meet the requirements of current- and voltage-mode MLF filter design, a multiple input and multiple output CMOS OTA with high frequency capability, low-voltage/low-power operation, sufficient transconductance tuning range and low excess phase is proposed. The proposed OTA is based on source degeneration topology. The simulation is carried

out using standard TSMC 0.18μm CMOS. The large signal analysis shows that the transconductance can be easily tuned by changing the gate voltage of degeneration transistors. Using a single 2V supply voltage, 150MHz cut-off frequency and less than 15mW power consumption were obtained for current-mode seventh-order 0.05° equiripple linear phase OTA-C lowpass filter with only manual fine adjustments (without on-chip tuning) of transconductances and pre-distortion of circuit capacitor values. In particular, reasonable group delay ripple (the key design specification) has been achieved, although it was previously reported that MLF based OTA-C filters suffer from relatively large group delay errors. Thus, the current-mode FLF filter can be expected to be suitable for portable electronic systems, especially for hard disk read/write channels with inclusion of a practical automatic tuning circuit. Design of a voltage-mode 400MHz IFLF linear phase filter using the same OTA with 2.5V supply voltage has also been investigated. The filter phase response of the seventh-order IFLF filter is fairly linear; the filter group delay ripple up to cut-off frequency is approximately 6%, which is slightly higher than the minimum read channel filter specification (≤5%). This is mainly due to parasitic effects and internal nodes of the OTA. The group delay ripple can be further improved by decreasing the widths of OTA input stage and increasing the widths of OTA output stage, but decreasing the widths of the OTA input stage will reduce the transconductance value and increasing the widths of the output stage will increase power consumption and chip area. Therefore, there are tradeoffs between the group delay ripple, power consumption and chip area. The next generation HDD read channel also requires larger gain boost. However, the group delay ripple will be increases as the gain boost is increased; therefore, the gain boost tends to be realized in digital domain. The simulation results have shown clearly that even with a relatively higher supply voltage, the MLF IFLF and FLF configurations still have lower power consumption than many other filters in the literature. MLF IFLF and FLF configurations can be a useful alternative of linear phase filtering for next generation HDD read channels.

4. Synthesis and Design of Current-mode MLF LF OTA-C Filters with Application in HDD Read Channels

4.1 Introduction

The MLF LF structure is no doubt one of the most popular choices in CT filter design [1]. It has some obvious advantages compared with other structures such as the cascade, MLF FLF and IFLF [54], especially in terms of sensitivity and is widely used for high performance filter applications with stringent requirements [118-127]. Traditional filter designs based on the LF structure are too complex, as they are based on the simulation of passive RLC ladder prototypes [1, 120-122] or using a MLF theory [1, 123, 124]. The RLC ladder simulation approach requires some good knowledge of passive RLC filters and the active simulation process, whilst the MLF approach involves non-trivial matrix manipulation. Furthermore, none of the two methods has simple explicit design formulas for LF active filters and the RLC ladder based method also has restriction on realizable zeros. A general transfer function may be realized using the direct signal flow graph (SFG) method [106]. The resulting filters have either the regular FLF or IFLF configuration or also simple explicit design formulas. However, the direct SFG method is not suitable for the LF filter design. While simple explicit formulas do exist for the FLF and IFLF configurations based on the MLF method [105-107] and the SFG method [108], an iterative complex process is required for the LF synthesis. Straightforward explicit formulas for the most often used orders of the most attractive LF filters are needed for ready use. Very recently, synthesis of voltage-mode LF OTA-C filters has been conducted [127]. In this chapter we present three current-mode filter structures using the LF configuration and derive simple explicit formulas for the realization of arbitrary filter characteristics using these structures. Thus, the next section of this chapter, Section 4.2, the synthesis of all-pole current-mode LF configuration is derived. The input distribution system is

added to the all-pole configuration is introduced in Section 4.3. In Section 4.4, the output summation system is also derived. Section 4.5 presents the design of seventh-order 0.05° equiripple lowpass filter by using MLF LF output summation system. Finally, the discussion and conclusions are given in Section 4.6.

4.2 All-pole Current-mode LF Feedback OTA-C Filters

The general all-pole LF feedback OTA-C filter configuration [118, 119] is shown in Figure 4.1. It has the minimum number of components and uses only grounded capacitors. With time constant $\tau_j = C_j/g_j$, by inspection we can write the equations of the circuit as

$$\begin{aligned}
I_{o1} &= (I_{input} - I_{o1} - I_{o2})/\tau_1 s, \\
I_{o2} &= (I_{o1} - I_{o3})/\tau_2 s, \\
I_{oj} &= (I_{o(j-1)} - I_{o(j+1)})/\tau_j s, \\
I_{o(n-1)} &= (I_{o(n-2)} - I_{on})/\tau_{n-1} s, \\
I_{on} &= I_{o(n-1)}/\tau_n s \\
I_{output} &= I_{on}
\end{aligned} \tag{4.1}$$

where I_{input} is the overall input current and I_{output} is the overall output current of the filter respectively, I_{oj} is the output current of the j_{th} integrator and s is the complex frequency.

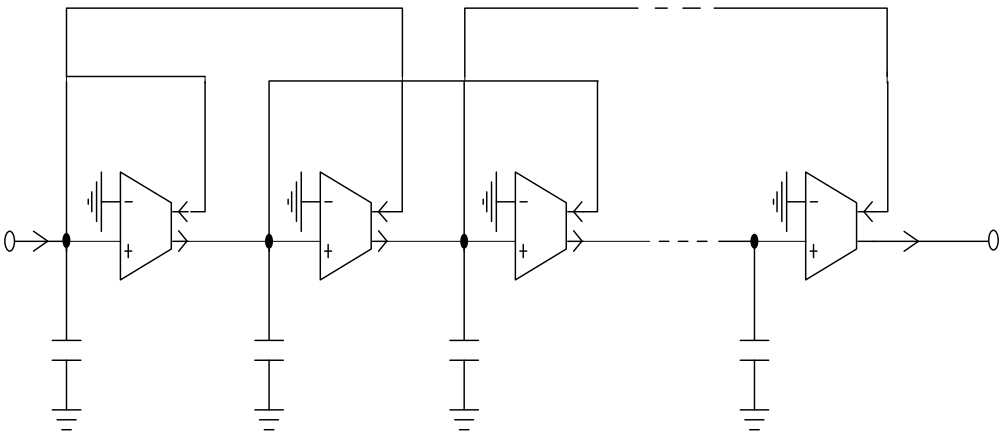


Figure 4.1 General all-pole current-mode MLF LF OTA-C configuration

The overall transfer function $H(s)$ of the LF filter in Figure 4.1 can be derived using equation (4.2) as

$$H(s) = \frac{I_{output}}{I_{input}} = \frac{1}{D(s)} \tag{4.2}$$

where the denominator polynomial *D(s)* of respective overall transfer functions for *n* = 3 to 6 are given below.

n=3:

$$D(s) = \tau_1\tau_2\tau_3 s^3 + \tau_2\tau_3 s^2 + (\tau_1 + \tau_3)s + 1$$

n=4:

$$D(s) = \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_3\tau_4)s^2 + (\tau_2 + \tau_4)s + 1$$

n=5:

$$\begin{aligned} D(s) = {} & \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3 \\ & + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1 \end{aligned}$$

n=6:

$$\begin{aligned} D(s) = {} & \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 + \tau_2\tau_3\tau_4\tau_5\tau_6 s^5 + (\tau_1\tau_2\tau_3\tau_4 + \tau_1\tau_2\tau_3\tau_6 + \tau_1\tau_2\tau_5\tau_6 + \\ & \tau_1\tau_4\tau_5\tau_6 + \tau_3\tau_4\tau_5\tau_6)s^4 + (\tau_2\tau_3\tau_4 + \tau_2\tau_3\tau_6 + \tau_2\tau_5\tau_6 + \tau_4\tau_5\tau_6)s^3 + \\ & (\tau_1\tau_2 + \tau_1\tau_4 + \tau_1\tau_6 + \tau_3\tau_4 + \tau_3\tau_6 + \tau_5\tau_6)s^2 \\ & + (\tau_2 + \tau_4 + \tau_6)s + 1 \end{aligned} \tag{4.3}$$

To realise the general unity DC gain all-pole transfer function

$$H_d(s) = \frac{1}{B_n s^n + B_{n-1} s^{n-1} + \cdots + B_1 s + 1} \tag{4.4}$$

The explicit expressions for determining parameter values can be obtained from the coefficient matching equations based on the comparison between the coefficients of $H(s)$ and those in equation (4.3). The following are the derived design formulas.

n=3:

$$\tau_1 = \frac{B_3}{B_2}, \quad \tau_2 = \frac{B_2}{B_1 - \tau_1}, \quad \tau_3 = B_1 - \tau_1$$

n=4:

$$\tau_1 = \frac{B_4}{B_3}, \quad \tau_2 = \frac{B_3}{B_2 - B_1\tau_1}, \quad \tau_3 = \frac{B_2 - B_1\tau_1}{B_1 - \tau_2}, \quad \tau_4 = B_1 - \tau_2 \tag{4.5}$$

n=5:

$$\tau_1 = \frac{B_5}{B_4}, \quad \tau_2 = \frac{B_4}{B_3 - B_2\tau_1}, \quad \tau_3 = \frac{B_3 - B_2\tau_1}{B_2 - (B_1 - \tau_1)\tau_2}, \quad \tau_4 = \frac{B_2 - (B_1 - \tau_5)\tau_2}{B_1 - \tau_1 - \tau_3},$$
$$\tau_5 = B_1 - \tau_1 - \tau_3$$

n=6:

$$\tau_1 = \frac{B_6}{B_5}, \quad \tau_2 = \frac{B_5}{B_4 - B_3\tau_1}, \quad \tau_3 = \frac{B_4 - B_3\tau_1}{B_3 - (B_2 - B_1\tau_1)\tau_2}, \quad \tau_4 = \frac{B_3 - (B_2 - B_1\tau_1)\tau_2}{B_2 - (B_1 - \tau_2)\tau_3 - B_1\tau_1},$$

$$\tau_5 = \frac{B_2 - (B_1 - \tau_2)\tau_3 - B_1\tau_1}{B_1 - \tau_2 - \tau_4}, \quad \tau_6 = B_1 - \tau_2 - \tau_4$$

In the above the synthesis of the general all-pole LF structure has been presented. In the following we will present the general MLF LF OTA-C structures with transmission zeros. Arbitrary transmission zeros are realized by using either an input distributor or an output summer [107, 127]. The filter transfer functions and design formulas of the respective structures will be formulated.

4.3 Current-mode LF MLF OTA-C Filters with Input Distributor

The desired general transfer functions in equation. (4.6) can be realised by adding an input distribution OTA network to the all-pole LF structure in Figure 4.1 to produce zeros.

$$H_d(s) = \frac{A_n s^n + A_{n-1} s^{n-1} + \cdots + A_1 s + A_0}{B_n s^n + B_{n-1} s^{n-1} + \cdots + B_1 s + 1} \tag{4.6}$$

The resultant general current-mode LF OTA-C filter structure is shown in Figure 4.2.

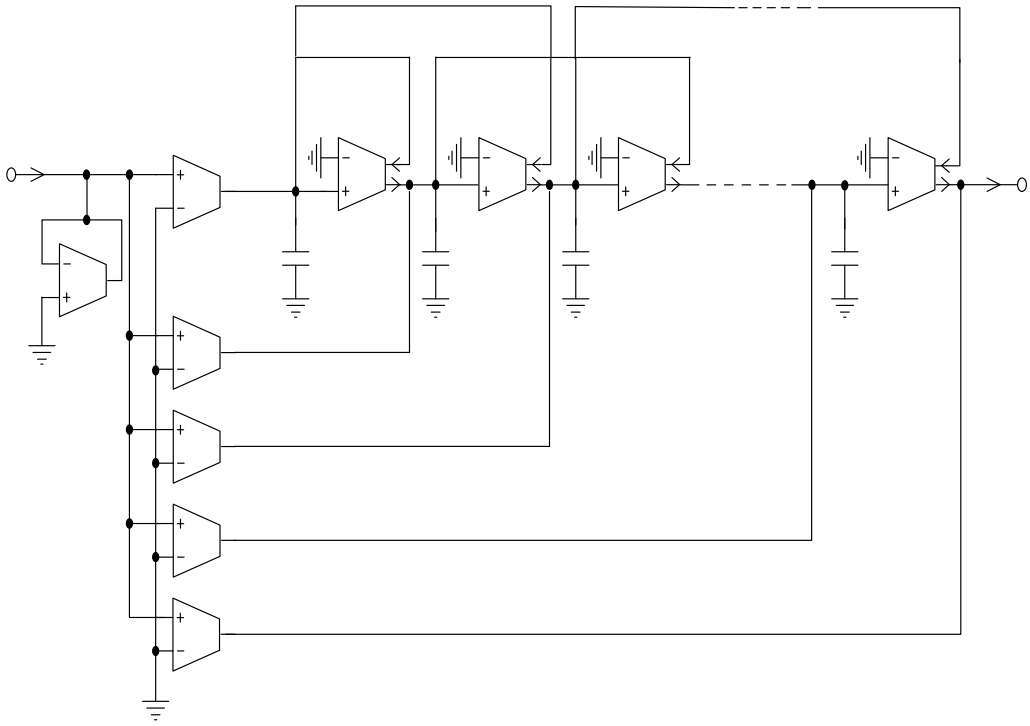


Figure 4.2 Universal current-mode LF OTA-C filter structures with input distribution OTA network.

Denoting $\beta_j = g_{\beta j}/g_r$, the circuit equations of the filter in Figure 4.3 can be written as

$$\begin{aligned}
I_{o1} &= (\beta_1 I_{input} - I_{o1} - I_{o2})/\tau_1 s, \\
I_{o2} &= (\beta_2 I_{input} + I_{o1} - I_{o3})/\tau_2 s, \\
I_{oj} &= (\beta_j I_{input} + I_{o(j-1)} - I_{o(j+1)})/\tau_j s, \\
I_{o(n-1)} &= (\beta_{n-1} I_{input} + I_{o(n-2)} - I_{on})/\tau_{n-1} s, \\
I_{on} &= (\beta_n I_{input} + I_{o(n-1)})/\tau_n s \\
I_{output} &= \beta_{(n+)} I_{input} + I_{on}
\end{aligned} \tag{4.7}$$

I. input

Using the equations in equation (4.7), we can derive the numerators $N(s)$ of the transfer functions and the corresponding explicit design formulas to determine the distribution parameters β_j, when realizing the general function in equation (4.8) for

g.

order n = 3 to 6, as:

n=3:

$$N(s)=\beta_4\tau_1\tau_2\tau_3 s^3+(\beta_3\tau_1\tau_2+\beta_4\tau_2\tau_3)s^2+[\beta_4(\tau_1+\tau_3)+\beta_3\tau_2+\beta_2\tau_1]s+(\beta_1+\beta_2+\beta_3+\beta_4)$$

$$\beta_4=A_3/B_3,\quad \beta_3=(A_2-\beta_4B_2)/\tau_1\tau_2,\quad \beta_2=(A_1-\beta_4B_1-\beta_3\tau_2)/\tau_1,\quad \beta_1=A_0-(\beta_2+\beta_3+\beta_4)$$

n=4:

$$N(s)=\beta_5\tau_1\tau_2\tau_3\tau_4 s^4+(\beta_4\tau_1\tau_2\tau_3+\beta_5\tau_2\tau_3\tau_4)s^3+[\beta_5(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4)+\beta_4\tau_2\tau_3+\beta_3\tau_1\tau_2)s^2$$
$$+[\beta_5(\tau_2+\tau_4)+\beta_4(\tau_1+\tau_3)+\beta_3\tau_2+\beta_2\tau_1]s+(\beta_1+\beta_2+\beta_3+\beta_4+\beta_5)$$

$$\beta_5=A_4/B_4,\quad \beta_4=(A_3-\beta_5B_3)/\tau_1\tau_2\tau_3,\quad \beta_3=(A_2-\beta_5B_2-\beta_4\tau_2\tau_3)/\tau_1\tau_2,$$
$$\beta_2=[A_1-\beta_5B_1-\beta_4(\tau_1+\tau_3)-\beta_3\tau_2]/\tau_1,\quad \beta_1=A_0-(\beta_2+\beta_3+\beta_4+\beta_5)$$

n=5:

$$N(s)=\beta_6\tau_1\tau_2\tau_3\tau_4\tau_5 s^5+(\beta_6\tau_2\tau_3\tau_4\tau_5+\beta_5\tau_1\tau_2\tau_3\tau_4)s^4+[\beta_6(\tau_1\tau_2\tau_3+\tau_1\tau_2\tau_5+\tau_1\tau_4\tau_5+\tau_3\tau_4\tau_5)$$
$$+\beta_4\tau_1\tau_2\tau_3+\beta_5\tau_2\tau_3\tau_4]s^3+[\beta_6(\tau_2\tau_3+\tau_2\tau_5+\tau_4\tau_5)+\beta_5(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4)+\beta_4\tau_2\tau_3+\beta_3\tau_1\tau_2]s^2$$
$$+[\beta_6(\tau_1+\tau_3+\tau_5)+\beta_5(\tau_2+\tau_4)+\beta_4(\tau_1+\tau_3)+\beta_3\tau_2+\beta_2\tau_1]s+(\beta_1+\beta_2+\beta_3+\beta_4+\beta_5+\beta_6)$$

$$\beta_6=A_5/B_5,\quad \beta_5=(A_4-\beta_6B_4)/\tau_1\tau_2\tau_3\tau_4,\quad \beta_4=(A_3-\beta_6B_3-\beta_5\tau_2\tau_3\tau_4)/\tau_1\tau_2\tau_3,$$
$$\beta_3=[A_2-\beta_6B_2-\beta_5(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4)-\beta_4\tau_2\tau_3]/\tau_1\tau_2,$$
$$\beta_2=[A_1-\beta_6B_1-\beta_5(\tau_2+\tau_4)-\beta_4(\tau_1+\tau_3)-\beta_3\tau_2]/\tau_1,\quad \beta_1=A_0-(\beta_2+\beta_3+\beta_4+\beta_5+\beta_6)$$

n=6:

$$N(s)=\beta_7\tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6+(\beta_6\tau_1\tau_2\tau_3\tau_4\tau_5+\beta_7\tau_2\tau_3\tau_4\tau_5\tau_6)s^5+[\beta_7(\tau_1\tau_2\tau_3\tau_4+\tau_1\tau_2\tau_3\tau_6+\tau_1\tau_2\tau_5\tau_6$$
$$+\tau_1\tau_4\tau_5\tau_6+\tau_3\tau_4\tau_5\tau_6)+\beta_5\tau_1\tau_2\tau_3\tau_4+\beta_6\tau_2\tau_3\tau_4\tau_5]s^4+[\beta_7(\tau_2\tau_3\tau_4+\tau_2\tau_3\tau_6+\tau_2\tau_5\tau_6+\tau_4\tau_5\tau_6)$$
$$+\beta_6(\tau_1\tau_2\tau_3+\tau_1\tau_2\tau_5+\tau_1\tau_4\tau_5+\tau_3\tau_4\tau_5)+\beta_4\tau_1\tau_2\tau_3+\beta_5\tau_2\tau_3\tau_4]s^3+[\beta_7(\tau_1\tau_2+\tau_1\tau_4+\tau_1\tau_6+\tau_3\tau_4$$
$$+\tau_3\tau_6+\tau_3\tau_5)+\beta_6(\tau_2\tau_3+\tau_2\tau_5+\tau_4\tau_5)+\beta_5(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4)+\beta_3\tau_1\tau_2+\beta_4\tau_2\tau_3]s^2+[\beta_7(\tau_2+\tau_4+\tau_6)$$
$$+\beta_6(\tau_1+\tau_3+\tau_5)+\beta_5(\tau_2+\tau_4)+\beta_4(\tau_1+\tau_3)+\beta_2\tau_1+\beta_3\tau_2]s+(\beta_1+\beta_2+\beta_3+\beta_4+\beta_5+\beta_6+\beta_7)$$

$$\beta_7=A_6/B_6,\quad \beta_6=(A_5-\beta_7B_5)/\tau_1\tau_2\tau_3\tau_4\tau_5,\quad \beta_5=(A_4-\beta_7B_4-\beta_6\tau_2\tau_3\tau_4\tau_5)/\tau_1\tau_2\tau_3\tau_4,$$
$$\beta_4=[A_3-\beta_7B_3-\beta_6(\tau_1\tau_2\tau_3+\tau_1\tau_2\tau_5+\tau_1\tau_4\tau_5+\tau_3\tau_4\tau_5)-\beta_5\tau_2\tau_3\tau_4]/\tau_1\tau_2\tau_3,$$
$$\beta_3=[A_2-\beta_7B_2-\beta_6(\tau_2\tau_3+\tau_2\tau_5+\tau_4\tau_5)-\beta_5(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4)-\beta_4\tau_2\tau_3]/\tau_1\tau_2,$$
$$\beta_2=[A_1-\beta_7B_1-\beta_6(\tau_1+\tau_3+\tau_5)-\beta_5(\tau_2+\tau_4)-\beta_4(\tau_1+\tau_3)-\beta_3\tau_2]/\tau_1,$$
$$\beta_1=A_0-(\beta_2+\beta_3+\beta_4+\beta_5+\beta_6+\beta_7)$$

Note that the denominators of the corresponding transfer functions have already been given in Section 4.2 and the design formulas for the pole parameters τ_j of the respective orders have also been given in equation (4.3). Also, if the maximum order in the numerator is required to be n-1, then we can remove the $g_{a(n+1)}$ OTA and simply output the current I_{on} directly. For realization of specific filter characteristics the output OTA network may be simplified accordingly.

4.4 Current-mode LF OTA-C Lowpass Filters with Output Summation

Similarly, by adding the output summation OTA network to the all-pole LF structure in Figure 4.1 the general transfer function in equation (4.6) can be realised and the resulting current-mode LF OTA-C filter structure is shown in Figure 4.3.

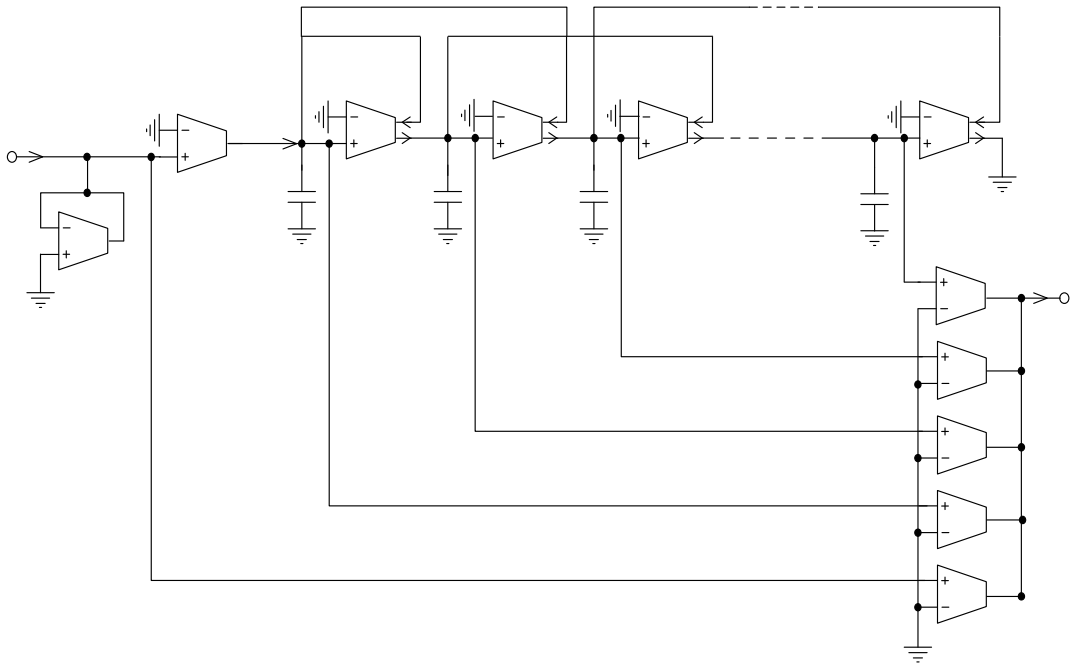


Figure 4.3 Universal current-mode MLF LF OTA-C filter structures with output summation OTA network

Denoting $\alpha_j=g_{\alpha j}/g_j$, $\gamma=g_0/g_\gamma$ we can attain the circuit equations of the filter in Figure 4.3 as shown below.

$$
\begin{aligned}
I_{o1} &= (\gamma I_{input} - I_{o1} - I_{o2})/\tau_1 s,\\
I_{o2} &= (I_{o1} - I_{o3})/\tau_2 s,\\
I_{oj} &= (I_{o(j-1)} - I_{o(j+1)})/\tau_j s,\\
I_{o(n-1)} &= (I_{o(n-2)} - I_{on})/\tau_{n-1} s,\\
I_{on} &= I_{o(n-1)}/\tau_n s\\
I_{output} &= \alpha_0 \gamma I_{input} + \sum_{i=1}^{n} (\alpha_i I_{oi})
\end{aligned}
\tag{4.8}
$$

Using equation (4.8) we can derive the numerators $N(s)$ of the transfer functions and the corresponding explicit design formulas of summation parameters α_j when realizing the general function in equation (4.3) for order n = 3 to 6, given below.

n=3:

$$N(s) = \alpha_0\tau_1\tau_2\tau_3 s^3 + (\alpha_0+\alpha_1)\tau_2\tau_3 s^2 + [\alpha_0(\tau_1+\tau_3) + \alpha_2\tau_3]s + (\alpha_0+\alpha_1+\alpha_3)$$

$$\alpha_0 = A_3/B_3, \quad \alpha_1 = A_2/B_2 - \alpha_0, \quad \alpha_2 = (A_1 - \alpha_0 B_1)/\tau_3, \quad \alpha_3 = A_0 - (\alpha_0+\alpha_1)$$

n=4:

$$
\begin{aligned}
N(s) = \alpha_0\tau_1\tau_2\tau_3\tau_4 s^4 + (\alpha_0+\alpha_1)\tau_2\tau_3\tau_4 s^3 + [\alpha_0(\tau_1\tau_2+\tau_1\tau_4+\tau_3\tau_4) + \alpha_2\tau_3\tau_4]s^2\\
+ [(\alpha_0+\alpha_1)(\tau_2+\tau_4) + \alpha_3\tau_4]s + (\alpha_0+\alpha_2+\alpha_4)
\end{aligned}
$$

$$
\begin{aligned}
\alpha_0 = A_4/B_4, \quad \alpha_1 = A_3/B_3 - \alpha_0, \quad \alpha_2 = (A_2 - \alpha_0 B_2)/\tau_3\tau_4,\\
\alpha_3 = [A_1 - \alpha_0 B_1 - \alpha_1(\tau_2+\tau_4)]/\tau_4, \quad \alpha_4 = A_0 - (\alpha_1+\alpha_2)
\end{aligned}
$$

n=5:

$$
\begin{aligned}
N(s) = \alpha_0\tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + (\alpha_0+\alpha_1)\tau_2\tau_3\tau_4\tau_5 s^4 + [\alpha_0(\tau_1\tau_2\tau_3+\tau_1\tau_2\tau_5+\tau_1\tau_4\tau_5+\tau_3\tau_4\tau_5)\\
+ \alpha_2\tau_3\tau_4\tau_5]s^3 + [(\alpha_0+\alpha_1)(\tau_2\tau_3+\tau_2\tau_5+\tau_4\tau_5) + \alpha_3\tau_4\tau_5]s^2\\
+ [\alpha_0(\tau_1+\tau_3+\tau_5) + \alpha_2(\tau_3+\tau_5) + \alpha_4\tau_5]s + (\alpha_0+\alpha_1+\alpha_3+\alpha_5)
\end{aligned}
$$

$$
\begin{aligned}
\alpha_0 = A_5/B_5, \quad \alpha_1 = A_4/B_4 - \alpha_0, \quad \alpha_2 = (A_3 - \alpha_0 B_3)/\tau_3\tau_4\tau_5,\\
\alpha_3 = [A_2 - (\alpha_0+\alpha_1)B_2 - \alpha_1 B_2]/\tau_4\tau_5,\\
\alpha_4 = [A_1 - \alpha_0 B_1 - \alpha_2(\tau_3+\tau_5)]/\tau_5, \quad \alpha_5 = A_0 - (\alpha_0+\alpha_1+\alpha_3)
\end{aligned}
$$

n=6:

$$N(s)=\alpha_0\tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6+(\alpha_0+\alpha_1)\tau_2\tau_3\tau_4\tau_5\tau_6 s^5$$
$$+[\alpha_0(\tau_1\tau_2\tau_3\tau_4+\tau_1\tau_2\tau_3\tau_6+\tau_1\tau_2\tau_5\tau_6+\tau_1\tau_4\tau_5\tau_6+\tau_3\tau_4\tau_5\tau_6)+\alpha_2\tau_3\tau_4\tau_5\tau_6]s^4$$
$$+[(\alpha_0+\alpha_1)(\tau_2\tau_3\tau_4+\tau_2\tau_3\tau_6+\tau_2\tau_5\tau_6+\tau_4\tau_5\tau_6)+\alpha_3\tau_4\tau_5\tau_6]s^3$$
$$+[(\alpha_0+\alpha_2)(\tau_3\tau_4+\tau_3\tau_6+\tau_5\tau_6)+\alpha_0(\tau_1\tau_2+\tau_1\tau_4+\tau_1\tau_6)+\alpha_4\tau_5\tau_6]s^2$$
$$+[(\alpha_0+\alpha_1)(\tau_2+\tau_4+\tau_6)+\alpha_3(\tau_4+\tau_6)+\alpha_5\tau_6]s+(\alpha_0+\alpha_2+\alpha_4+\alpha_6)$$

$$\alpha_0=A_6/B_6,\quad \alpha_1=A_5/B_5-\alpha_0,\quad \alpha_2=(A_4-\alpha_0B_4)/\tau_3\tau_4\tau_5\tau_6,$$
$$\alpha_3=[A_3-(\alpha_0+\alpha_1)B_3]/\tau_4\tau_5\tau_6,$$
$$\alpha_4=[A_2-\alpha_0B_2-\alpha_2(\tau_3\tau_4+\tau_3\tau_6+\tau_5\tau_6)]/\tau_5\tau_6,$$
$$\alpha_5=[A_1-(\alpha_0+\alpha_1)B_1-\alpha_3(\tau_4+\tau_6)]/\tau_6,\quad \alpha_6=A_0-(\alpha_0+\alpha_2+\alpha_4)$$

Again note that the denominators of the corresponding transfer functions have been given in Section 4.2 and design formulas for the τ_j of the respective orders can be determined using equation (4.3). Also, Note that if the maximum order in the numerator is required to be n-1, then we can remove the g_{a0}, g_0, and g_r OTAs and the input current can be applied to the input of the first integrator directly. For realization of specific transmission zeros the OTAs in the output network may not be all necessary.

4.5 Design of Current-mode Seventh-Order 0.05° Equiripple Linear Phase OTA-C Lowpass Filter using LF Output Summation

The voltage–mode LF filter structure has been used in [36, 37]. However, in [36], only the single-ended structure was implemented and the group delay ripple is about 7%. In [37], the group delay ripple is less than 5%, but the speed is low and power consumption is high. In last section, the current-mode FLF structure have been investigated for equalizers, but the group delay ripple is not quite satisfied, due to the hard to control feedback. Therefore, we design another high performance equalizer based on current-mode LF configuration for HDD systems in this section. In section 4.5.1, the filter synthesis of seventh-order current-mode LF configuration is derived.

In order to increase the speed of equalizer, the simply OTA is needed. Therefore, a modified simple OTA is presented in section 4.5.2. In section 4.5.3, we present the detail simulation results of the proposed high performance equalizer.

4.5.1 The Synthesis of Current-mode Seventh-order 0.05° Equiripple Linear Phase OTA-C LF Filter

To realize the following desired lowpass characteristic with zeros, for example,

$$H_d(s) = \frac{A_2 s^2 + A_0}{B_7 s^7 + B_6 s^6 + B_5 s^5 + B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + 1} \tag{4.9}$$

The current-mode LF OTA-C filter structure with output summation OTAs shown in Figure 4.4 can be utilized.

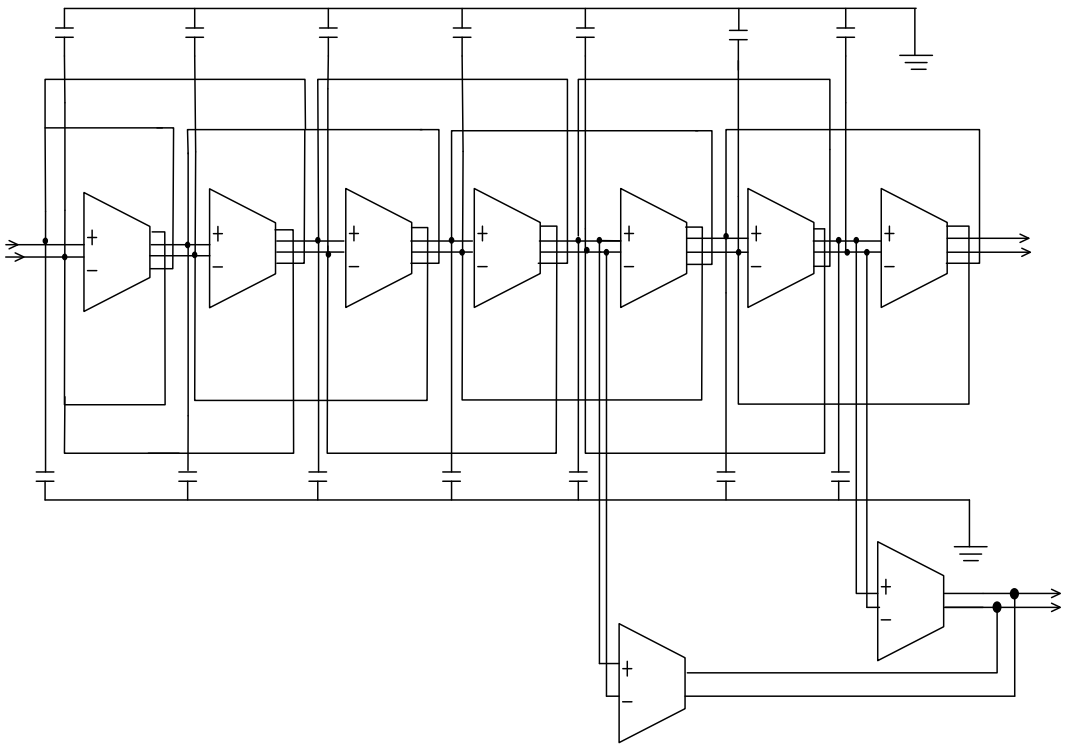


Figure 4.4 Seventh-order current-mode LF OTA-C filters with output summation network

The overall transfer function of the circuit can be obtained as:

$$H(s) = \frac{I_{output}}{I_{input}} = \frac{N(s)}{D(s)} \tag{4.10}$$

where

$$N(s) = \alpha_5 \tau_6 \tau_7 s^2 + (\alpha_5 + \alpha_7)$$

$$\begin{aligned} D(s) = {} & \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^6 + (\tau_1\tau_2\tau_3\tau_4\tau_5 + \tau_1\tau_2\tau_3\tau_4\tau_7 + \tau_1\tau_2\tau_3\tau_6\tau_7 + \tau_1\tau_2\tau_5\tau_6\tau_7 \\ & + \tau_1\tau_4\tau_5\tau_6\tau_7 + \tau_3\tau_4\tau_5\tau_6\tau_7) s^5 + (\tau_2\tau_3\tau_4\tau_5 + \tau_2\tau_3\tau_4\tau_7 + \tau_2\tau_3\tau_6\tau_7 + \tau_2\tau_5\tau_6\tau_7 + \tau_4\tau_5\tau_6\tau_7) s^4 \\ & + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_2\tau_7 + \tau_1\tau_4\tau_5 + \tau_1\tau_4\tau_7 + \tau_1\tau_6\tau_7 + \tau_3\tau_4\tau_5 + \tau_3\tau_4\tau_7 + \tau_3\tau_6\tau_7 + \tau_5\tau_6\tau_7) s^3 \\ & + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_2\tau_7 + \tau_4\tau_5 + \tau_4\tau_7 + \tau_6\tau_7) s^2 + (\tau_1 + \tau_3 + \tau_5 + \tau_7) s + 1 \end{aligned}$$

The design formulas of the filter can be attained by coefficient matching between equation (4.9) and equation (4.10) as:

$$\begin{gathered} \tau_1 = \frac{B_7}{B_6}, \quad \tau_2 = \frac{B_6}{B_5 - B_4\tau_1}, \quad \tau_3 = \frac{B_5 - B_4\tau_1}{B_4 - (B_3 - B_2\tau_1)\tau_2}, \\ \tau_4 = \frac{B_4 - (B_3 - B_2\tau_1)\tau_2}{B_3 - B_2\tau_1 - [B_2 - (B_1 - \tau_1)\tau_2]\tau_3}, \quad \tau_5 = \frac{B_3 - B_2\tau_1 - [B_2 - (B_1 - \tau_1)\tau_2]\tau_3}{B_2 - (B_1 - \tau_1 - \tau_3)\tau_4 - (B_1 - \tau_1)\tau_2}, \\ \tau_6 = \frac{B_2 - (B_1 - \tau_1 - \tau_3)\tau_4 - (B_1 - \tau_1)\tau_2}{B_1 - \tau_1 - \tau_3 - \tau_5}, \quad \tau_7 = B_1 - \tau_1 - \tau_3 - \tau_5, \\ \alpha_5 = \frac{A_2}{\tau_6\tau_7}, \quad \alpha_7 = A_0 - \alpha_5 \end{gathered} \tag{4.11}$$

For the normalized characteristic of a seventh-order lowpass 0.05° equiripple linear phase filter with real zeros at the cut-off frequency, we have [1]

$$\begin{gathered} A_2 = -A_0 = 1, \quad B_7 = 0.055617, \quad B_6 = 0.291094, \quad B_5 = 1.095656, \\ B_4 = 2.554179, \quad B_3 = 4.255922, \quad B_2 = 4.676709, \quad B_1 = 3.176156 \end{gathered}$$

Using equation (4.11), the pole and zero parameters τ's and α's can be computed as:

$$\begin{gathered} \tau_1 = 0.19106, \quad \tau_2 = 0.47905, \quad \tau_3 = 0.64409, \quad \tau_4 = 0.74214, \quad \tau_5 = 0.84224, \\ \tau_6 = 1.00706, \quad \tau_7 = 1.49877, \quad \alpha_5 = 0.662536, \quad \alpha_7 = 0.337464 \end{gathered} \tag{4.12}$$

Further design can be conducted based on these results. For example, we can assign $g_7 = g_6 = g_5 = g_4 = g_3 = g_2 = g_1$. Using the computed parameter values given in

equation (4.12), the g_{aj}, and C_j values can be calculated using $g_{aj} = g_j\alpha$ and $C_j = g_j\tau_j$ respectively.

The grounded capacitance can then be calculated as:

$$C_1 = 0.3646\ pF,\ C_2 = 0.1403\ pF, C_3 = 1.5848\ pF, C_4 = 1.9989\ pF,$$
$$C_5 = 2.1185\ pF, C_6 = 2.5624\ pF, C_7 = 3.8868\ pF$$

4.5.2 Transistor-level OTA Design

The use of small load capacitors is advisable, even the parasitic capacitors are typically larger than these values. The time constant τ is equal to C/g, increasing the total transconductance value can reduce the parasitic effect but it costs many amount of power. Decreasing the total transconductance value can achieve minimum power consumption. However, the parasitic effects can be critical in some circumstances. Moreover, such as noise, THD, DR needs to be considered as well. Fortunately, for HDD applications, DR need not be very high, typically 40dB is sufficient and requirement on DC gain is also not stringent due to the low-Q operation. In this design, a simple one-stage OTA based on source degeneration topology and without internal nodes is thus utilized as shown in Figure 4.5 [39, 41], mainly to meet the UHF requirement.

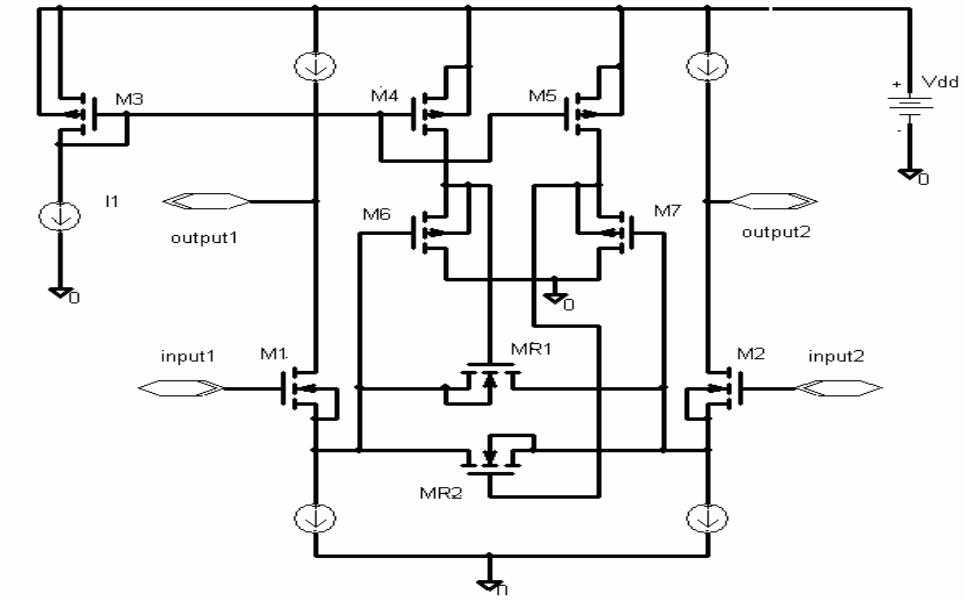


Figure 4.5 The simulated unit OTA

In this section, the following square-law equation is used:

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_T)^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L}(V_{DSAT})^2 \tag{4.13}$$

where, μ_n and C_{ox} are the mobility of the carriers in the channel and gate-source capacitance per square, respectively. V_{DSAT} is the saturation voltage, and W and L are the width and length of the transistor gate, respectively. For the structures shown in Figure 4.5, the small signal transconductance is approximately given by:

$$I_{out} = \frac{g_{m1}}{N+1} \sqrt{1 - [\frac{V_{in}}{2V_{DSAT}(N+1)}]^2} \tag{4.14}$$

Therefore, the OTA low-frequency small signal transconductance is:

$$G_m = \frac{g_{m1}}{N+1} \tag{4.15}$$

where g_{m1} is matched with g_{m2} is the low-electric-field transconductance of the differential pair. N is the source degeneration factor. The two degenerated transistors M_{R1} and M_{R2} can be tuned by bias current I_1, in order to achieve different transconductance. If the second order effects are taken into account, the source degeneration factor will be modified as:

$$N \cong \frac{g_{m1} + g_{mb1}[1 + K_{R1}R_{sx}(V_{GS1} - V_{Tn})]}{K_{R1}(V_{GSR1} - V_{Tn})} + K_{R1}R_{sx}(V_{GS1} - V_{Tn}) \tag{4.16}$$

where $\theta \cdot (V_{GS1} - V_{Tn})$ accounts for the mobility degradation of the NMOS devices. An ideal square-law MOSFET has a resistance R_{sx} in series with the source, the θ can be modelled as $\mu_0 C_{ox}(W/L)R_{sx}$ and $g_{mb1,2}$ models the body effects. K is equal to $\mu_n C_{OX}(W/L)$. As shown in equation (4.16), the larger θ the larger N. However, the larger N leads the smaller G_m. While source degeneration factor reduces the overall transconductance, the output impedance is boosted by the same factor. In fact, there is a cascode effect inherently present in the source degenerated topologies.

4.5.3 Simulation Results

The filter circuit in Figure 4.4 was simulated using the component values designed in section 4.5.1 and the OTA in Figure 4.5 using BSIM 3v3 Spice models for a TSMC 0.18μm CMOS process [112, 113]. With 2.5V supply voltage and terminate the OTA with short-circuit, simulated DC responses of the OTA are shown in Figures 4.6.

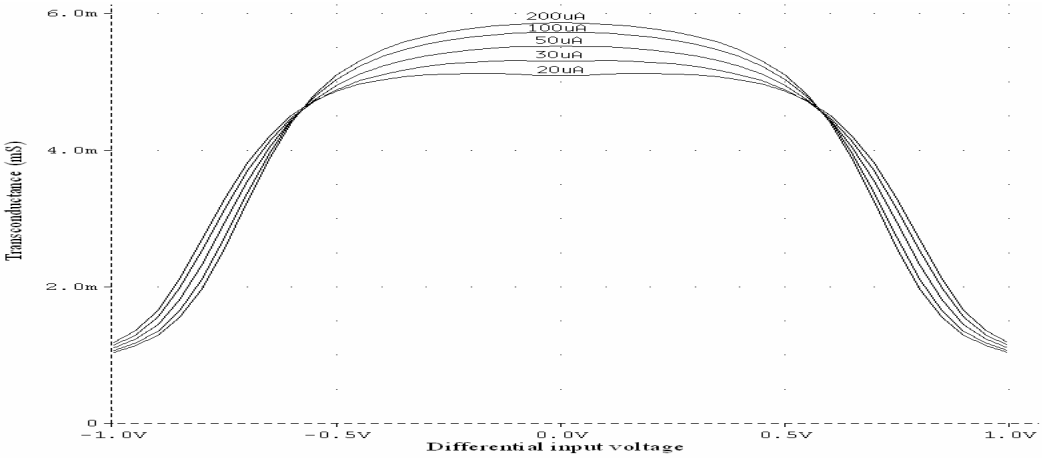


Figure 4.6 Simulated DC transconductance versus differential input voltage for varying bias voltages of the OTA with short-circuit load

The simulated open-circuit cut-off frequencies of the OTA cell are presented in Figure 4.7.

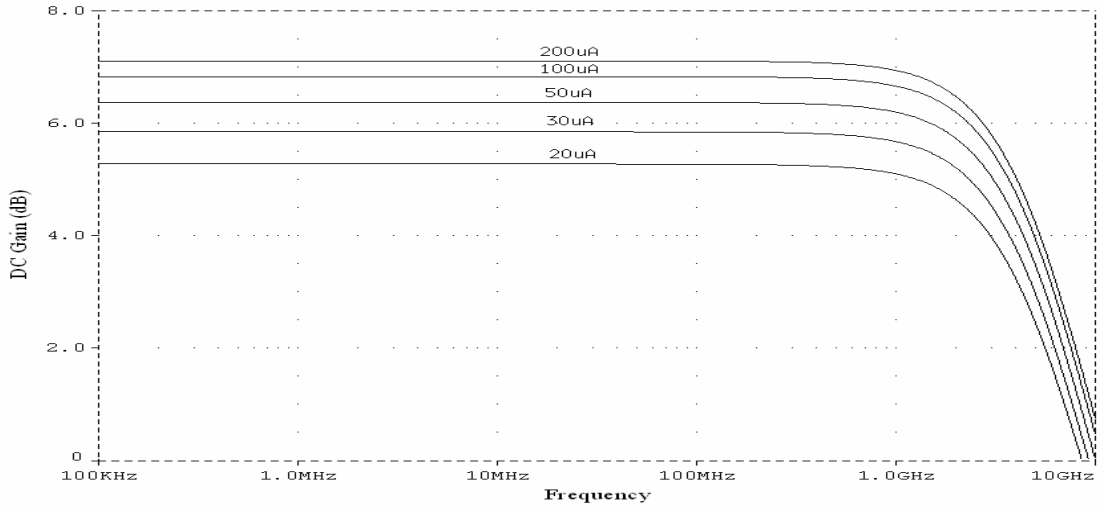


Figure 4.7 Simulated AC open-circuit frequency responses of the OTA with different bias currents

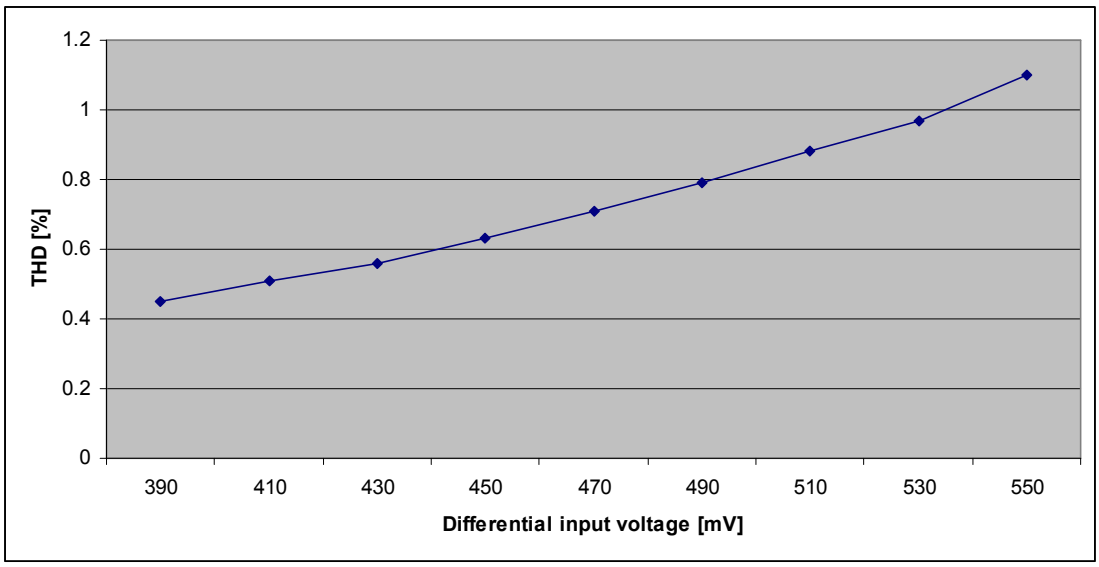


Figure 4.8 Simulated THD as a function of differential input voltage of the OTA in Figure 4.5

Less than 1% THD can be guaranteed for the differential input voltage of less than 530mV.

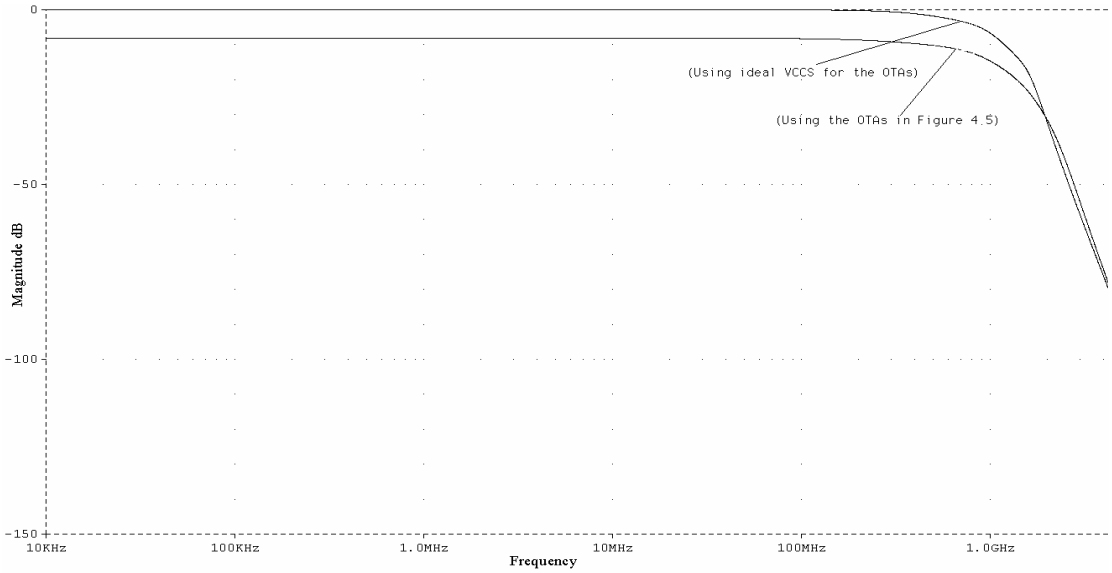


Figure 4.9 Simulated magnitude response of the current-mode LF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

The Figure 4.9 shows the simulated magnitude response of the filter with ideal VCCS

and OTA in Figure 4.5. It is shown that there is 9dB drop between using ideal VCCS and practical OTA simulation results at the passband of the proposed filter. It is because that the single stage OTA is used in Figure 4.5, which has low output resistance and leads low DC gain of the OTA. The group delay ripple of proposed filter with ideal VCCS and OTA in Figure 4.5 are also shown in Figure 4.10.

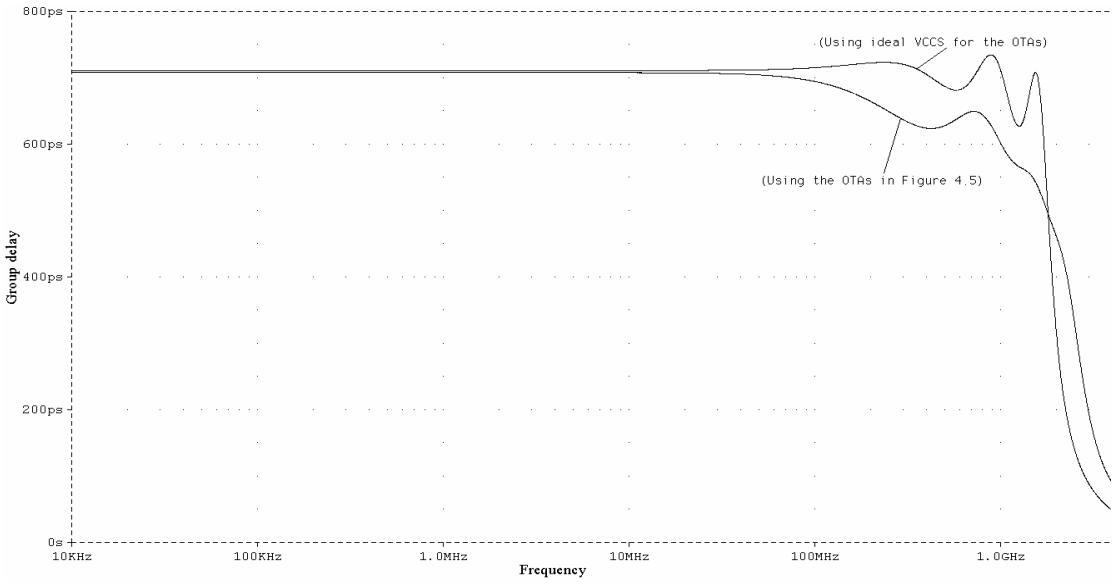


Figure 4.10 Simulated group delay response of the current-mode LF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

The group delay ripple of the lowpass filter without gain boost for $f_c/5 \leq f \leq 1.4\, f_c$ is approximately 5% over the whole tuning range. Although there is deviation between the ideal group delay ripple of the lowpass filter and that using the OTA in Figure 4.5, the group delay ripple of the lowpass filter using the OTA in Figure 4.5 is still less than 5%. Simulation results also show that the DR of the filter, defined as the RMS of the output current signal at 1% THD divided by the total RMS output noise current integrated over the bandwidth, which is $500nA_{RMS}$, is 54dB. The gain boost of the filter is about 10dB. Simulated THD versus differential input voltage and frequency are shown in Figures 4.11 and 4.12, respectively. The THD less than 1% is obtained for the differential input current up to 250mV and the frequency up to 675MHz.

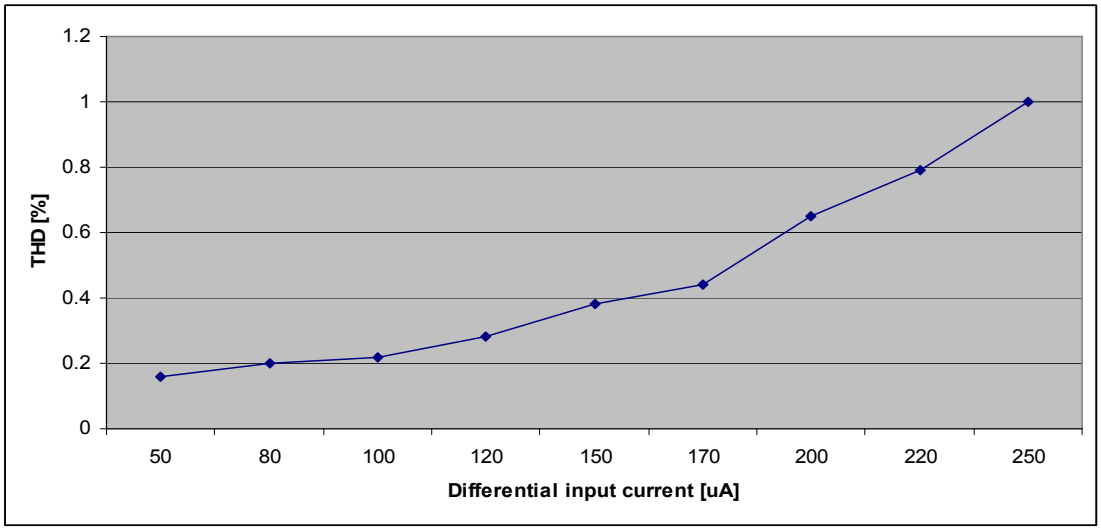


Figure 4.11 Simulated THD versus the differential input current of the current-mode LF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

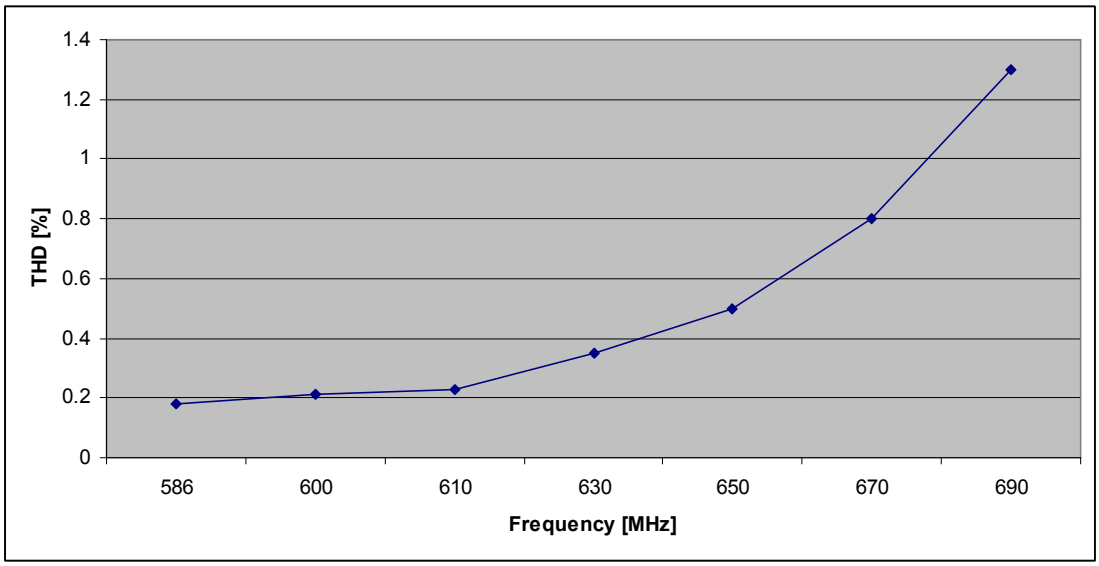


Figure 4.12 Simulated THD versus frequency of the current-mode LF seventh-order 0.05° equiripple linear phase OTA-C lowpass filter

As can also be seen from Figures 4.13 and 4.14, the mismatch of the input transistors affects both the filter magnitude frequency response and group delay. With 10% mismatch of the input transistors, the group delay ripple of the proposed filter does not remain less than 5%, which cannot be accepted for computer HDD read channels.

Therefore, on chip automatic tuning is needed to correct the effects due to process mismatch.

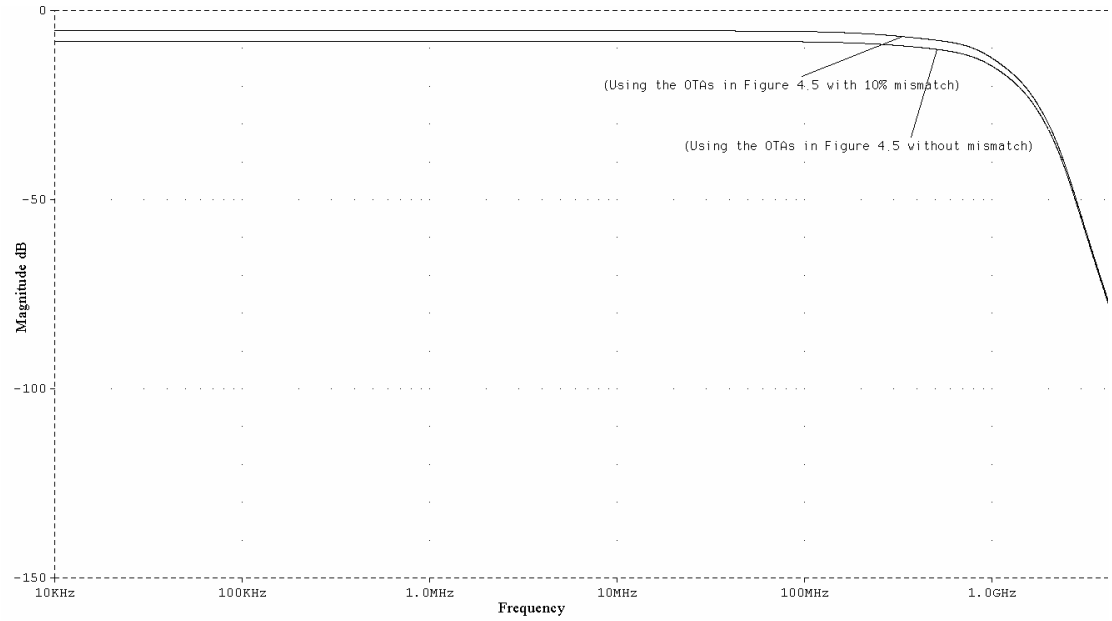


Figure 4.13 Simulated filter magnitude frequency responses with and without 10% mismatch

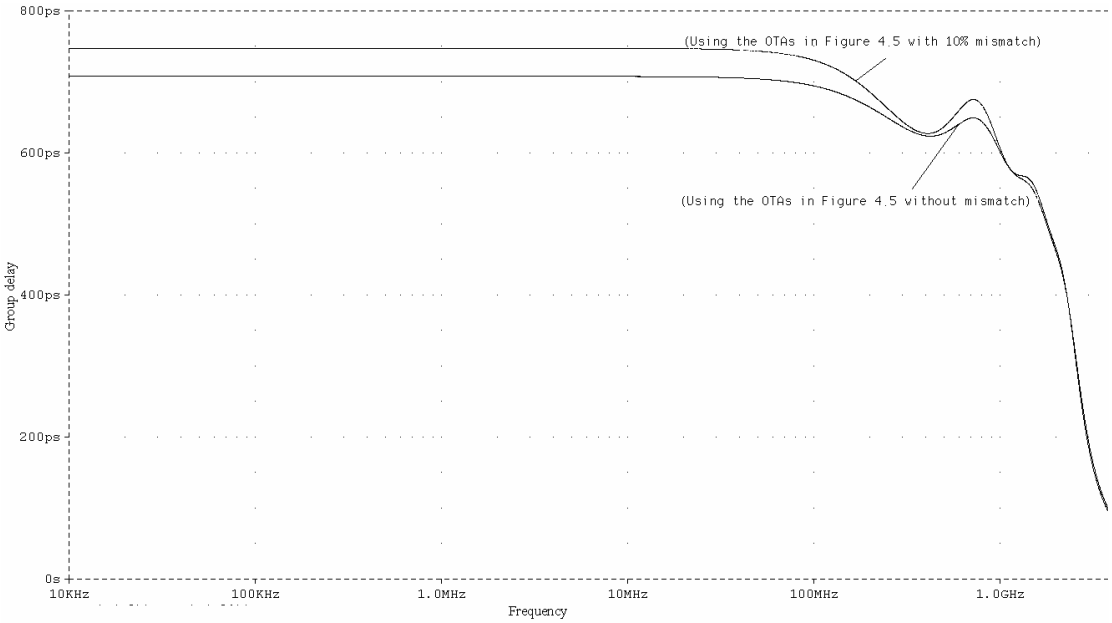


Figure 4.14 Simulated filter group delay response with and without 10% mismatch

The simulation also shows that varying the bias current I_1 of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 590-690MHz. The total power

consumption of the filter is about 370mW. The summary of proposed is given in Table 4.1.

Table 4.1 Simulated results of the current-mode seventh-order LF 0.05° equiripple linear phase lowpass filter based on a TSMC 0.18μm CMOS process

Nominal -3dB cut-off frequency	650MHz
Tunable -3dB cut-off frequency range	590-690 MHz
Group delay ripple	5% up to 1.4fc
Dynamic range (THD = 1%)	54dB
Gain boost range	0-10dB
Nominal power dissipation @ 2.5V	370mW

4.6 Conclusions

The synthesis and general performance analysis of low-sensitivity current-mode MLF LF OTA-C filters have been presented and design of an equalizer using the current-mode LF output-summation OTA-C filter structure for HDD read/write channel applications has been particularly investigated. The filter structures are canonical and do not have any node that is without any capacitor to ground. All-pole filters are realized using the basic current-mode LF structure and filters with arbitrary transmission zeros are established using either input distribution or output summation OTA networks. Unlike the synthesis based on the matrix method of MLF OTA-C filters that has been reported in [65], the demonstrated iterative synthesis approach does not require the knowledge of the general MLF theory. The explicit design formulas also derived (for n = 3, 4, 5, and 6) are simple and useful for quick design of LF based all-pole and arbitrary transmission zero filters without the need of re-formulation. In order to further demonstrate the proposed synthesis and structure, a current-mode seventh-order 0.05° equiripple OTA-C lowpass filter with a 650MHz nominal cut-off frequency has been designed with the presented OTA as a building

block. Simulation results in a 0.18μm CMOS process with a 2.5V supply have revealed that the filter can achieve 650MHz of cut-off frequency with maximum 10dB of gain boost; the group delay ripple is about 5%. The maximum total power consumption is 370mW. The filter results have also verified the functionality of the presented OTA in filter applications. Analysis has shown that CMOS OTA non-idealities affect the filter frequency performance. In actual IC filter design, on-chip tuning circuitry is used to compensate the filter response deviations caused by the OTA non-idealities. Although no tuning was used for the filter, it is emphasized that automatic tuning schemes are important. They can reduce filter group delay ripple as well as filter performance deviation caused by the effects due to the process variations and device mismatch in MOS transistors of the OTAs.

5. Design and Simulation of Fifth-order 0.05° Equiripple Linear Phase MLF LF OTA-C Lowpass Filters for HDD Read Channels

5.1 Introduction

The fifth-order and seventh-order current-mode 0.05° equiripple linear phase lowpass filters based on current-mode LF, FLF configurations and voltage-mode IFLF configuration have been described in Chapter 4 and 3, respectively. It has shown that LF configuration has better group delay responses than FLF and IFLF ones. Therefore, the LF configuration has received more attention in past a few years. However, the current-mode FLF and voltage-mode IFLF configuration can achieve relatively lower power consumption than LF ones. Therefore, there is a trade-off between group delay ripple performance and power consumption. The extensive research has been doing on HDD read channels by using MLF structures recently [54-60]. Although the current-mode FLF and voltage-mode IFLF configuration can achieve some good performances and may be one of the filtering solutions for next generation HDD system, it is too hard to push the data rates to even further due to their global feedback loops introduce hard-to-minimize phase errors and parasitic effects. The HDD systems are high performance systems and support near real-time applications [45], which continue to develop at a rapid and deterministic pace to meet the emerging demands of high performance computing and peripheral devices. Moreover, the industrial are seeking for the solutions for next generation HDD read channels, the data rate is up to 2Gb/s at least. Thus a filter, whose cut-off frequency with at least 750MHz is demanding.

On the other hand, portable consumer electronics embedded with HDD chipsets have been getting more and more popular. Power consumption, supply voltage and chip area are all critical factors and bring along with many advantages as well as challenges in the design of these high-performance HDD chipsets. Low power

consumption helps to increase the battery lifetime and to reduce the operating temperature, which means performance of whole system is more stable due to less electrical parameter shift. Heat sinks can also be shrunk or even removed, which results in smaller dimension and lower cost. However, challenges lie in compensating the degradation in the performance, in order to meet the system specifications. In the digital domain, dynamic power decreases quadratically with supply voltage. On the contrary, analogue circuits typically need to consume more power at a lower supply voltage in order to maintain the same performance, because the large bias current may be needed to adjust the transistor in active region. Using the same low supply voltage for both analogue and digital part reduces the overall power consumption and also reduces the complexity of the interface. Unfortunately, the scaling down of threshold voltage does not follow the drop in the nominal supply voltage. As the available voltage headroom becomes limited, many existing circuit techniques in analogue domain cannot be applied. This chapter, therefore our design is targeted for fifth-order 0.05° equiripple linear phase OTA-C lowpass filter, which has cut-off frequency of 750MHz with minimized power consumption with accurate linear phase and gain boost.

This chapter is organized in the following way. The transistor-level design of the fully-differential OTA is discussed in Section 5.2. Filter architecture and synthesis of current- and voltage-mode filters are described in Section 5.3. The simulation results are given in Section 5.4, and finally conclusions are given in Section 5.5.

5.2 Transistor-level OTA Design

The performances of filter are not only relying on the filter structure, but also rely strongly on the performances of OTA. Therefore, the design of high-performances OTA is very demand. The source degeneration OTAs have received more attention than any other techniques based OTA due to the trade-offs between the linearity and power consumption [39-41, 47, 50, 51]. However, it has to pay the expense of the reduced overall transconductance. Moreover, the tuning range of the source

degeneration OTA relies strongly on the triode region transistors and thus it leads relatively small tuning range. An alterative OTA therefore, which is shown in Figure 5.1, is present in this section to optimize the tuning, group delay and power consumption. The CMOS OTA in Figure 5.1 is used for the filter design. In the unit OTA cell, M_1 and M_2 are the input transistors. M_3–M_6 act as active biasing circuitry in such a way that the total current drawn by M_3–M_6 is required for larger signals. The active biasing shares the same bias current source with the differential pair M_1-M_2. When the signal amplitude is small, M_3 and M_4 are in saturation while M_5 and M_6 are in triode region. The M_3-M_6 branches remove some of the bias current. When the signal amplitude is positive and large, M_6 will become saturated and M_5 will be cut off. A smaller proportion of the total bias current will be drawn by M_3-M_6. This results in larger currents in M_1 and M_2 to compensate for the drop of the transconductance. The sizing of the transistors must be optimized for maximum linearity [115]. In addition, differential active loading [67] has been employed to achieve higher output impedance without increasing the dc voltage drop. In addition, the differential loading is made with two triode region transistors for better linearity.

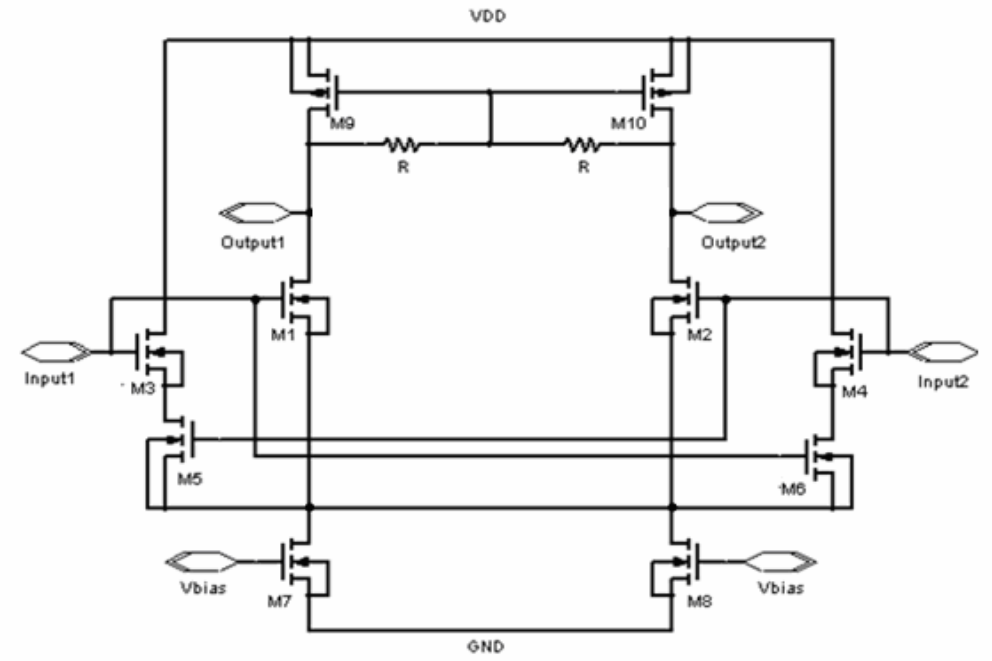


Figure 5.1 Fully-balanced unit OTA

In equation (5.1) the transistor works at triode region. The transistor works at active region is also expressed as equation (5.2).

$$I_D = \mu_n C_{ox}(\frac{W}{L})[(V_{GS} - V_T)\cdot V_{DS} - \frac{1}{2}V_{DS}^2]$$

(5.1)

$$I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_T)^2$$

(5.2)

We assume K_3 to be X times of K_5 and K_n equals to $\mu_n C_{OX}(W/L)$. The analysis starts form I_{D3} and I_{D5}:

$$I_{D3} = I_{D5} \Rightarrow X\cdot K_5(\frac{V_{in}}{2} - V_{D5} - V_T)^2 = 2K_5[-(\frac{V_{in}}{2} + V_{CM} + V_T)V_{DS5} - \frac{1}{2}V_{DS5}^2]$$

(5.3)

Let $V_{CM}+V_T=V_{CM}'$, the following relationship is obtained:

$$(X+1)V_{DS5}^2 - [(X-1)V_{in} - 2(X+1)V_{CM}']\cdot V_{DS5} + X(\frac{V_{in}}{2} - V_{CM}')^2 = 0$$

(5.4)

Therefore, the V_{DS5} is expressed below:

$$V_{DS5} = \frac{X-1}{2(X+1)}V_{in} - V_{CM}' + \frac{1}{2}\sqrt{[\frac{(X-1)V_{in} - 2(X+1)V_{CM}'}{X+1}]^2 - \frac{4X\cdot(\frac{V_{in}}{2} - V_{CM}')^2}{X+1}}$$

(5.5)

Then I_{D3} can be expressed as:

$$\begin{aligned} I_{D3} &= K_3[\frac{V_{in}}{2} - (V_{DS5} + V_{CM}')]^2 \\ &= \frac{K_3}{4(X+1)^2}[2V_{in} - \sqrt{(1-3X)V_{in}^2 + 4(X+1)V_{in}\cdot V_{CM}' + 4(X+1)V_{CM}'^2}]^2 \end{aligned}$$

(5.6)

I_{D4} has a similar expression, with V_{in} replaced by $-V_{in}$. Therefore, the $I_{D3}+I_{D4}$ are expressed as:

$$I_{D3}+I_{D4}=\frac{K_{3,4}}{2(X+1)^2}[(5-3X+4\sqrt{(X+1)})\cdot V_{in}^2+4(X+1)V_{cm}^{'2}]$$

(5.7)

The I_{D1}+I_{D2} are also expressed below:

$$I_{D1}+I_{D2}=2K_{1,2}[V_{CM}^{'2}+(\frac{V_{in}}{2})^2]$$

(5.8)

Therefore, the total current of I_{D1} *to* I_{D4} can then be expressed as:

$$\sum_{n=1}^{4}I_{Dn}=[\frac{K_{1,2}}{2}-\frac{K_{3,4}}{2(X+1)^2}(5-3X-4\sqrt{X+1})]V_{in}^2+2[K_{1,2}+(X+1)K_{3,4}]\cdot(V_{D5}+V_T)^2$$

(5.9)

In equation (5.9), the bias current is a given constant and the coefficient of V_{in}^2 depends on the size of the various transistors involved. If the coefficient of V_{in}^2 becomes zero, then the common source voltage becomes constant independently of the input voltage change.

$$I_{out}=K_{1,2}\sqrt{\frac{I_B-[\frac{K_{1,2}}{2}-\frac{K_{3,4}}{2(X+1)^2}(5-3X-4\sqrt{X+1})]V_{in}^2}{2[K_{1,2}+(X+1)K_{3,4}]}}V_{in}$$

(5.10)

Using Tyler series, then the equation (5.10) can be expanded as follow,

$$I_{out}\approx\sqrt{\frac{K_{1,2}^2I_B}{2[K_{1,2}+(X+1)K_{3,4}]}}V_{in}-\frac{K_{1,2}^2-\frac{K_{1,2}\cdot K_{3,4}}{(X+1)^2}(3X+4\sqrt{X+1}-5)}{12\sqrt{[K_{1,2}+(X+1)K_{3,4}]\cdot 2I_B}}V_{in}^3$$

(5.11)

Note that the even order harmonic distortions are ideally zero due to the symmetry of fully differential OTA. The total harmonic distortion is mainly determined by the third-order harmonic distortion (HD3). We may have a complete HD3 cancellation as long as the following condition is met,

$$K_{1,2}^{2} = \frac{K_{1,2} \cdot K_{3,4}}{(X+1)^2}(3X + 4\sqrt{X+1} - 5)$$

(5.12)

The above equation gives us an insight into how to design the OTA meeting the specification of linearity. Therefore, the transconductance of OTA can be expressed as:

$$G_m \approx \sqrt{\frac{K_{1,2}^{2} I_B}{2[K_{1,2} + (X+1)K_{3,4}]}}$$

(5.13)

5.2.1 Second-Order Effects of the OTA

Second-order effects, such as mobility reduction, body effect causing deviations from the ideal square-law behaviour of MOS devices have been neglected in the above analysis. However, high frequency filters require the use of high electric fields, thus the mobility reduction effects must also be taken into account. As a first order approximation, mobility reduction in MOS transistors may be modelled as,

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)}$$

(5.14)

where μ_0 is the zero-field mobility of carriers. An ideal square-law MOSFET has a resistance R_{sx} in series with the source [9]. θ is equal to $\mu_0 C_{ox}(W/L)R_{sx}$. On the other hand, the dependence on the bulk-source voltage resulting in body effect is another potential cause of nonlinear behaviour in the voltage-to-current conversion of the OTA in Figure 5.1. If the transistors are not connecting to V_{DD} or ground, the bulk-source voltages V_{BS} are not equal to zero and the threshold voltage can be expressed as,

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$$

(5.15)

where V_{T0} is the threshold voltage for V_{BS} is equal to zero, γ is the bulk threshold

parameter, and ø is the strong-inversion surface potential. Including the equation (5.14) in equation (5.15), the equation (5.13) can be approximated by equation (5.16),

$$G_m^{'} \approx \sqrt{\frac{K_{1,2} I_B}{\frac{1+K_{1,2}R_{sx}[V_{GS}-(V_{T0}+\gamma(\sqrt{\phi-V_{BS}}-\sqrt{\phi}))]}{2[\frac{(X+1)^3}{4\sqrt{X+1}+3X-5}+1]}}} \tag{5.16}$$

Thus, the mobility reduction limited the transconductance of the OTA.

5.2.2 Frequency Response of the OTA

Owing to the absence of internal nodes, the OTA in Figure 5.1 has excellent high-frequency performance. Figure 5.2 shows the small-signal model of the equivalent half-circuit of the OTA in Figure 5.1 with capacitive loads for frequency analysis. Using this model, the voltage transfer function of the OTA-C integrator can be shown as

$$A_v(s) = \frac{V_{out}(s)}{V_{id}(s)} = \frac{g_m}{s(C_L + C_p) + G_{out}} \tag{5.17}$$

where C_L and C_p are the load capacitance and parasitic output capacitance of the OTA, respectively, and G_{out} is the OTA's output conductance. The two parameters: C_p and G_{out} of the model are given by

$$\begin{aligned} C_p &= C_{DS1} + C_{DS9} + C_{GD1} + C_{GD9} \\ G_{out} &= g_{o1} + g_{o9} \end{aligned} \tag{5.18}$$

where g_{oi} is the output conductance of the MOS transistors of the OTA.

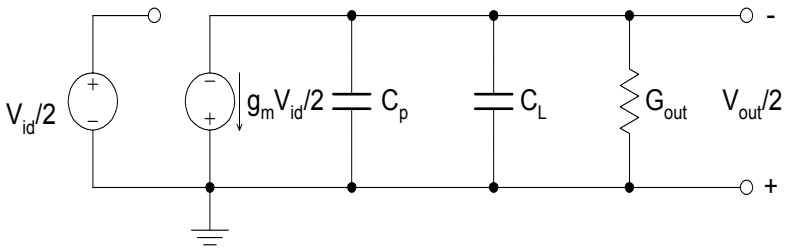


Figure 5.2 Small signal of Figure 5.1 with capacitive loads

From equation (5.17), the differential open-loop DC gain of the OTA can be obtained as:

$$A_{v0} = \frac{g_m}{G_{out}} \tag{5.19}$$

Equation (5.19) reveals that the OTA in Figure 5.1 does not have very high DC gain. We may see that the DC gain of the OTA can be increased by increasing either g_m or reducing G_{out}. G_m can be increased by increasing the *W/L* ratios of the input transistors. However, the DC drain currents of the input transistors are also increased proportionally, thus resulting in increased output conductance of the input transistors. Consequently, no significant increase in DC gain is expected. Moreover, the power consumption is increased as the *W/L* ratios are increased. Fortunately, the lowpass filter is low DC gain application, thus the moderate DC gain is enough to adjust the Q location. The OTA's bandwidth is determined by its dominant pole, which is located at the output nodes (as the highest impedance occurs at these nodes) and is approximately given by:

$$BW \approx f_d \approx \frac{G_{out}}{2\pi(C_L + C_p)} \tag{5.20}$$

where f_d is the dominant pole frequency of the OTA. Thus, the open-loop gain-bandwidth product of the OTA is the multiplication of equations (5.19) and (5.20).

$$GBW = \frac{g_m}{2\pi(C_L + C_p)} \tag{5.21}$$

Note that *BW* can be written as a function of *GBW* as

$$BW = \frac{GBW}{A_{v0}} \tag{5.22}$$

It is crucial to note that there is a trade-off between *BW* and A_{v0} as can be seen from equation (5.22). In other words, high bandwidth can be obtained at the expense of reduced DC gain and vice versa.

5.3 Design of Fifth-order 0.05° Equiripple Linear Phase LF OTA-C Lowpass Filter

The low power consumption designs of analogue circuits are challenging. The power consumption of analogue systems can be reduced by using low power supply voltage. However, it is not like digital systems design, the performance of analogue systems is relatively poor by using the advanced nanometres models such as 90nm, 60nm due to mismatch and noise issues. Therefore, the filter structure plays a very important role to reduce the power consumption. Certainly, the minimum power consumption can be achieved by using less number of OTAs. Therefore, cascade and MLF configurations have been widely used. However, the cascade configuration suffers from the high sensitivity, thus the MLF structures have been used for HDD application recently. They achieve good performance at very high frequency with filter are reduced parasitic effects and simple design methodologies. In last chapter, a current-mode seventh-order 0.05° equiripple linear phase OTA-C lowpass filter has been presented. The cut-off frequency of filter can be tuned up to 650MHz with large amount of power consumption. For next generation HDD read channels, not only the UHF is essential, but also the lower power consumption needs to be considered. Therefore, we propose fifth-order current- and voltage-mode 0.05° equiripple linear phase OTA-C lowpass filter based on LF configuration, which may be used for next generation HDD read channels.

5.3.1 Design of Current-mode Fifth-order 0.05° Equiripple Linear Phase LF OTA-C Lowpass Filter

The current-mode LF fifth-order OTA-C filter diagram is shown in Figure 5.3.

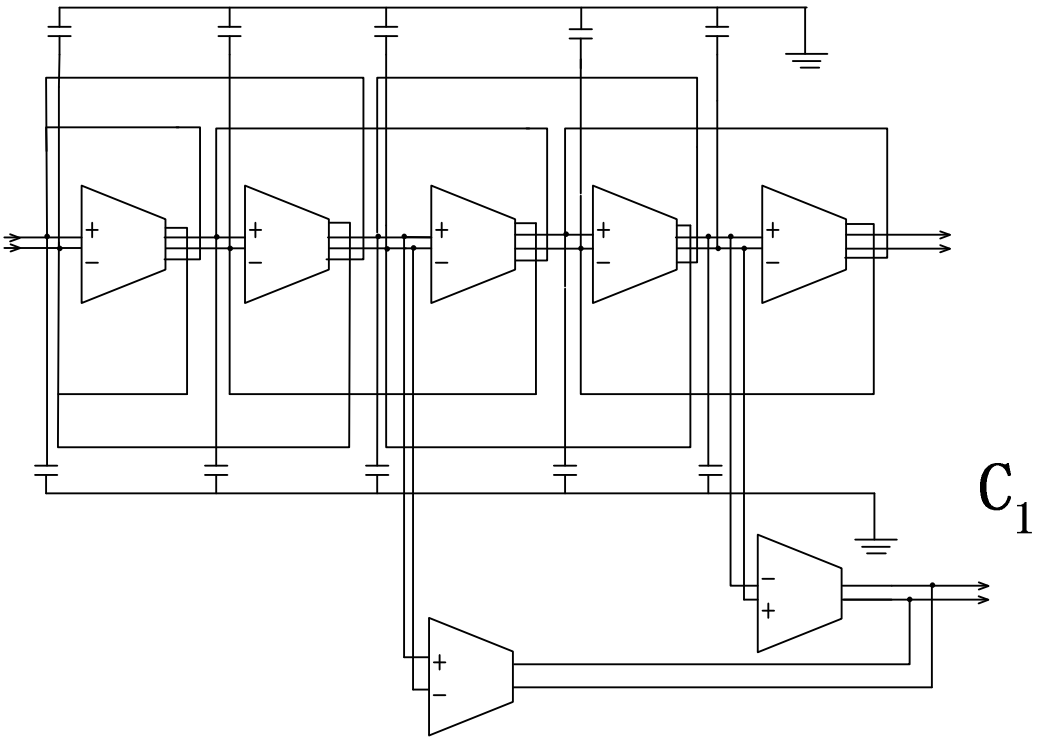


Figure 5.3 Fifth-order current-mode LF OTA-C lowpass filter with output summation network

For n=5, the design formulae of all-pole with output summation network were demonstrated in equation (4.3), (4.5) and (4.8):

$$H(s) = \frac{N(s)}{D(s)}$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1$$

$$N(s) = \alpha_3\tau_4\tau_5 s^2 + (\alpha_3 - \alpha_5)$$

The simplified design formulae for current-mode fifth-order 0.05° equiripple linear phase lowpass OTA-C filter are shown below:

$$\tau_1 = \frac{B_5}{B_4}, \tau_2 = \frac{B_4}{B_3 - B_2\tau_1}, \tau_3 = \frac{B_3 - B_2\tau_1}{B_2 - (B_1 - \tau_1)\tau_2}, \tau_4 = \frac{B_2 - (B_1 - \tau_1)\tau_2}{B_1 - \tau_1 - \tau_3}, \tau_5 = B_1 - \tau_1 - \tau_3,$$

$$\alpha_3 = \frac{A_2}{\tau_4\tau_5}, \alpha_5 = A_0 - \alpha_3$$

(5.23)

$$H_d(s) = \frac{(s^2 - 1)}{D_{d(s)}}$$

with

$$D_{d(s)} = 0.201926\ s^5 + 0.822285\ s^4 + 2.075924\ s^3 + 3.033116\ s^2 + 2.604527\ s + 1 \tag{5.24}$$

Using the coefficient matching between equations (5.23) and (5.24), the resulting pole $\tau_j = C_j/g_j$ and zero $\alpha_j = g_{aj}/g_j$ parameters can be calculated as:

$$\tau_1 = 0.24557\ , \tau_2 = 0.61776\ , \tau_3 = 0.84468\ , \tau_4 = 1.04066\ , \tau_5 = 1.51427\ ,$$
$$\alpha_3 = 0.36544\ , \alpha_5 = 0.63456$$

The filter is designed with identical unit OTAs using the CMOS OTA cell in Figure 5.1 to improve OTA matching and facilitate design automation. The cut-off frequency of the filter is chosen around 700MHz. Using the computed parameter values in above equations and choosing identical transconductances of 12mS for gj (j =1 to 5), the transconductances g_{a3} and g_{a5} can be calculated from above equation as 4.38mS and 7.61mS, respectively. The capacitor values can also be calculated, but the parasitic capacitance must also be taken into account. For the circuit of Figure 5.1, the parasitic capacitance is about 0.2pF. The capacitance and transconductance of zero OTAs values are recalculated below:

$$\begin{aligned} &C_1 = 1.14\ pF\ , C_2 = 3.171\ pF\ , C_3 = 4.4092\ pF\ , \\ &C_4 = 5.6786\ pF\ , C_5 = 8.063\ pF\ , \alpha_3 = 4.38\ mS\ , \\ &\alpha_5 = 7.61\ mS \end{aligned} \tag{5.25}$$

5.3.2 Design of Voltage-mode Fifth-order 0.05° Equiripple Linear Phase LF Lowpass OTA-C Filter

The voltage-mode LF lowpass OTA-C filter diagram is shown in Figure 5.4. For n=5, the design formulae of all-pole with input distribution networks were demonstrated in [55, 119, 127]:

$$D(s)=\tau_5\tau_4\tau_3\tau_2\tau_1 s^5+\tau_4\tau_3\tau_2\tau_1 s^4+(\tau_5\tau_4\tau_3+\tau_5\tau_4\tau_1+\tau_5\tau_2\tau_1+\tau_3\tau_2\tau_1)s^3$$
$$+(\tau_4\tau_3+\tau_4\tau_1+\tau_2\tau_1)s^2+(\tau_5+\tau_3+\tau_1)s+1$$

$$N(s)=\beta_3\tau_2\tau_1 s^2+(\beta_3-\beta_1)$$

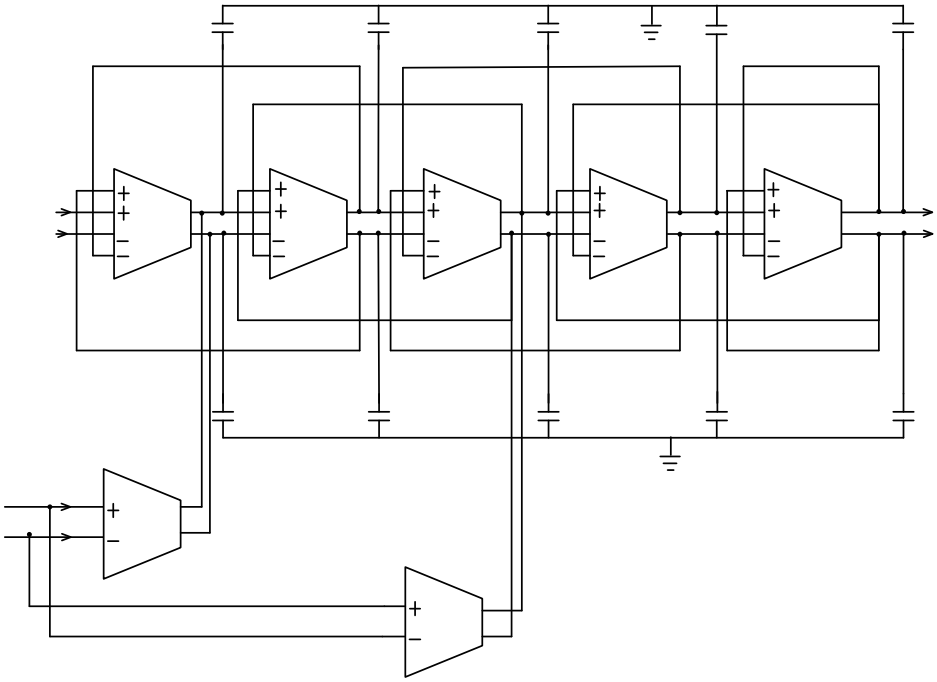


Figure 5.4 Fifth-order voltage-mode LF OTA-C lowpass filter with input distribution network

The simplified design formulae for voltage-mode fifth-order 0.05° equiripple linear phase OTA-C lowpass filter are shown below:

$$\tau_5=\frac{B_5}{B_4},\tau_4=\frac{B_4}{B_3-B_2\tau_5},\tau_3=\frac{B_3-B_2\tau_5}{B_2-(B_1-\tau_5)\tau_4},\tau_2=\frac{B_2-(B_1-\tau_5)\tau_4}{B_1-\tau_5-\tau_3},\tau_1=B_1-\tau_5-\tau_3,$$
$$\beta_3=\frac{A_2}{\tau_2\tau_1},\beta_1=A_0-\beta_3$$

(5.26)

Using the coefficient matching between equations (5.24) and (5.26), the resulting pole $\tau_j=C_j/g_j$ and zero $\beta_j=g_{\beta j}/g_j$ parameters can be calculated as:

$$\tau_5=0.24557\ ,\tau_4=0.61776\ ,\tau_3=0.84468\ ,\tau_2=1.04066\ ,\tau_1=1.51427\ ,$$
$$\beta_3=0.36544\ ,\beta_1=0.63456$$

a

g_1

b

Following the same procedure with last section, the capacitance, $g_{\beta 1}$, and $g_{\beta 3}$ values are also calculated below:

$$\begin{aligned} &C_5 = 1.14\ pF, C_4 = 3.171\ pF, C_3 = 4.4092\ pF, \\ &C_2 = 5.6786\ pF, C_1 = 8.063\ pF, g_{\beta 1} = 7.61\,mS, \\ &g_{\beta 3} = 4.38\,mS \end{aligned} \tag{5.27}$$

5.4 Simulation Results of Current- and Voltage-mode LF OTA-C Filters

5.4.1 Simulation Results of Transistor-level OTA

The OTA circuit was simulated using BSIM 3v3 Spice models for a 1.8V TSMC 0.18μm CMOS process available from MOSIS [112, 113]. The current-mode and voltage-mode filters circuits were simulated using the component values designed in section 5.3.1 and 5.3.2, respectively. The simulated OTA in Figure 5.1 is terminated by a short-circuit load. The simulated differential output current versus differential input voltage and DC transconductance versus differential input voltage for varying bias voltages of the OTA is shown in Figure 5.5 and 5.6, respectively.

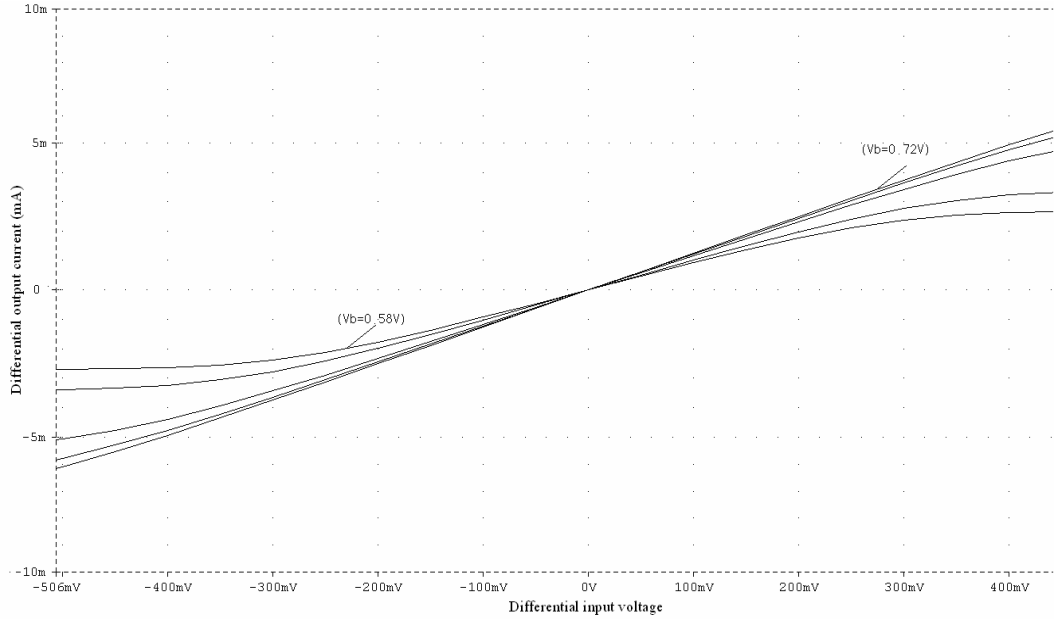


Figure 5.5 Simulated differential output current versus differential input voltage for varying bias voltages of the OTA with short-circuit load

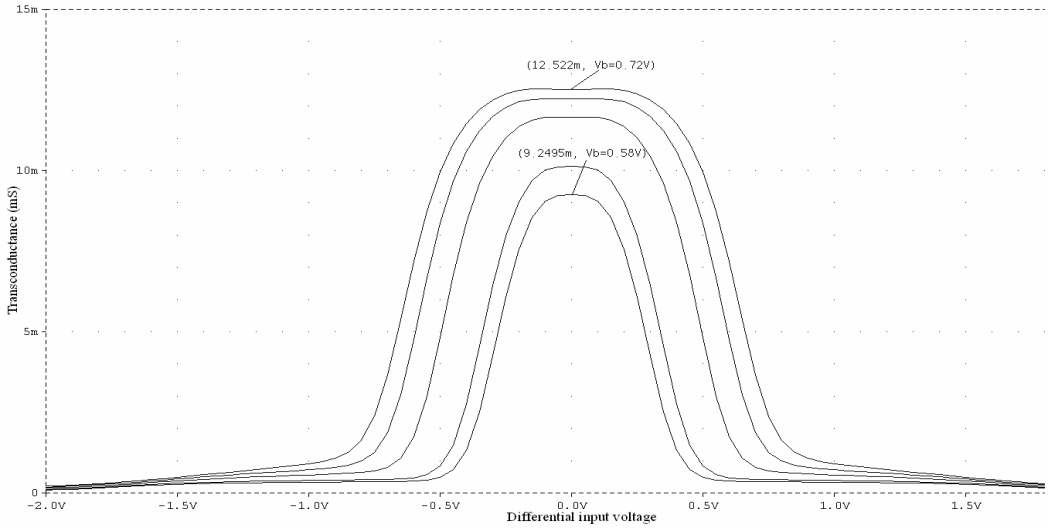


Figure 5.6 Simulated DC transconductance versus differential input voltage for varying bias voltages of the OTA with short-circuit load

The DC transconductance can be tuned from 9.2 to 12.5*mS* with 0.58V and 0.72V bias voltage. The simulated open-circuit cut-off frequencies of the OTA cell are also shown in Figure 5.7. The bandwidth of presented OTA is fairly large due to absence of internal node. Unity gain bandwidth can exceed 10GHz. However, the DC gain of presented OTA is relatively low due to the finite output resistance.

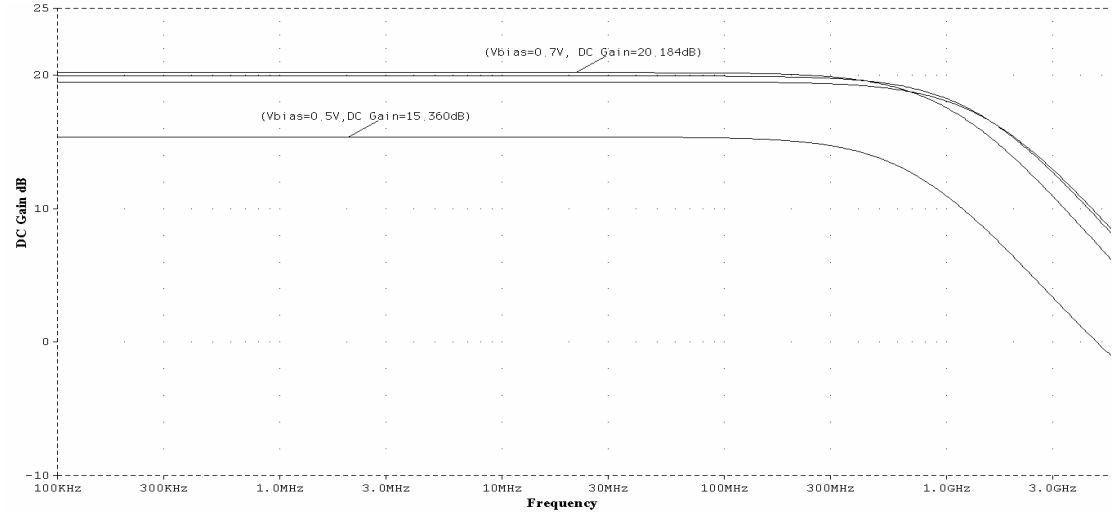


Figure 5.7 Simulated AC open-circuit frequency responses of the OTA with different bias currents

Figure 5.8 shows the THD as a function of differential input voltage of the OTA in

Figure 5.1. As can be seen, the THD is less than 1% for the differential input voltage up to 220mV.

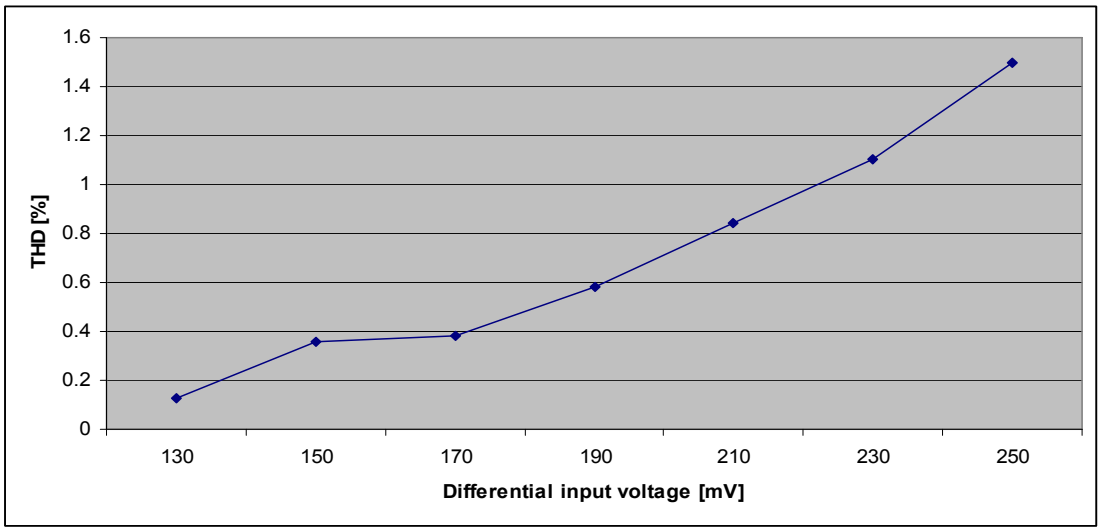


Figure 5.8 Simulated THD as a function of differential input voltage of the OTA in Figure 5.1

5.4.2. Simulation Results of Current-mode Fifth-order 0.05° Equiripple Linear Phase LF Lowpass OTA-C Filter

The magnitude responses of the presented filter using ideal VCCS and OTA in Figure 5.1 are shown in Figure 5.9.

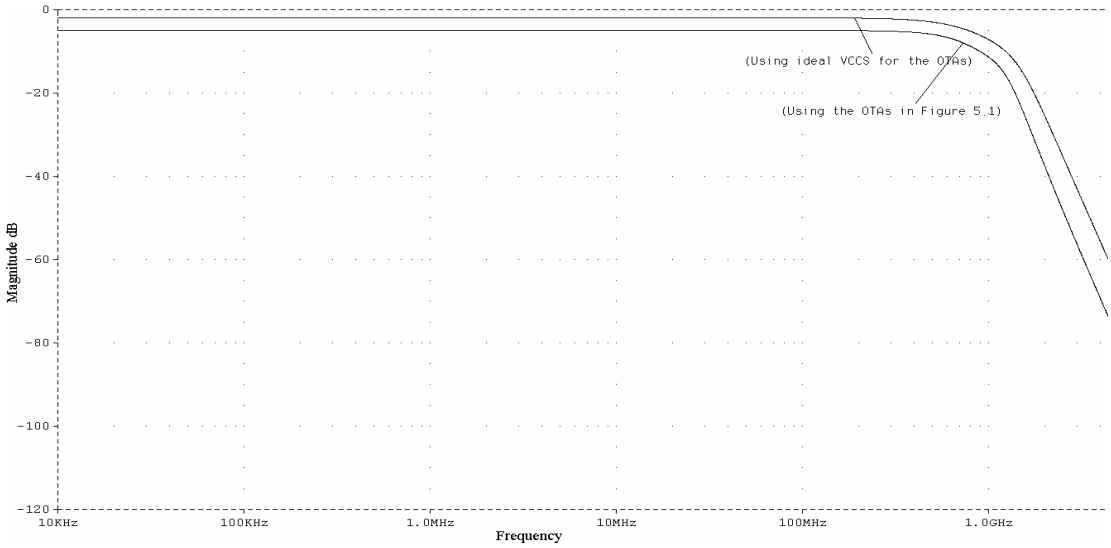


Figure 5.9 Simulated magnitude frequency responses of the current-mode LF fifth-order 0.05° equiripple linear phase lowpass OTA-C filter

As can be seen from Figure 5.9, the cut-off frequency of 720MHz is achieved by the filter. The 6dB gain boost of the filter is also realized by using output summation configuration.The filter phase responses are shown in Figure 5.10; the group delay ripple of the filter are fairly linear, although, using the OTA in Figure 5.1 causes 100ps group delay more than using ideal VCCS. As can also be seen, the ripple has very small variation up to 1.7 times of the cut-off frequency. The gain boost effects on the group delay ripples of filter due to the finite DC gain of the presented OTA, but the group delay ripple is still less than 5%. The filter's group delay ripple for $0 \leq f \leq 1.7f_c$ is approximately 4% with the group delay below ±25ps over the whole tuning range. This is well within the limit of the read channel filter specification.

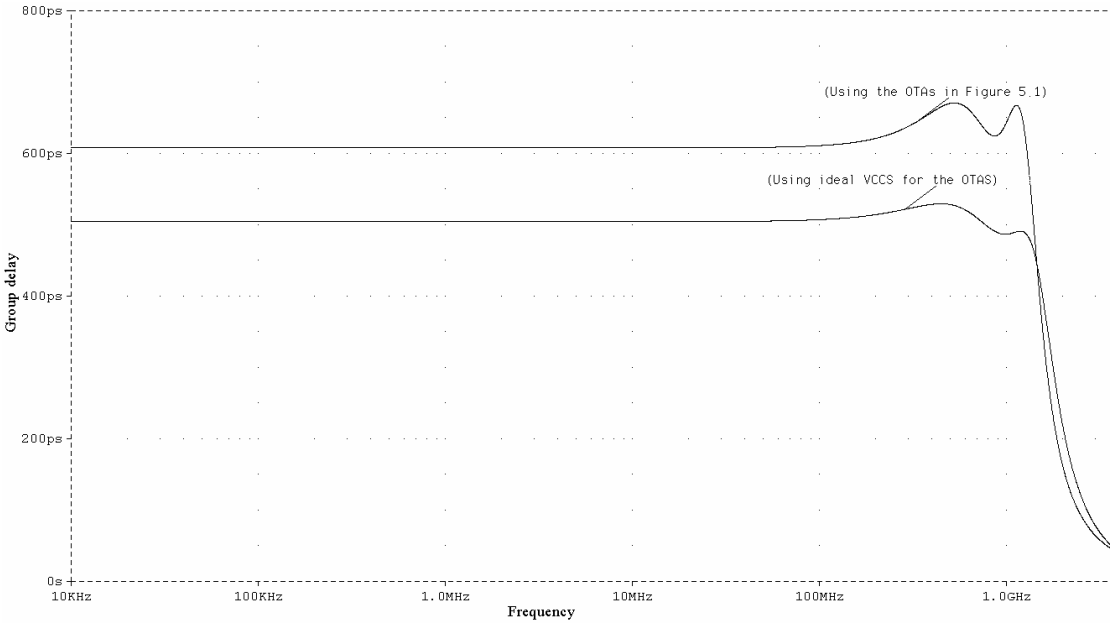


Figure 5.10 Simulated group delay responses of the current-mode LF fifth-order 0.05° equiripple linear phase OTA-C lowpass filter

The simulated THD as a function of differential input current and frequency are shown in Figures 5.11, 5.12, respectively. Less than 1% THD can be achieved for the input amplitude up to 870uA, and for the frequency up to 730MHz.

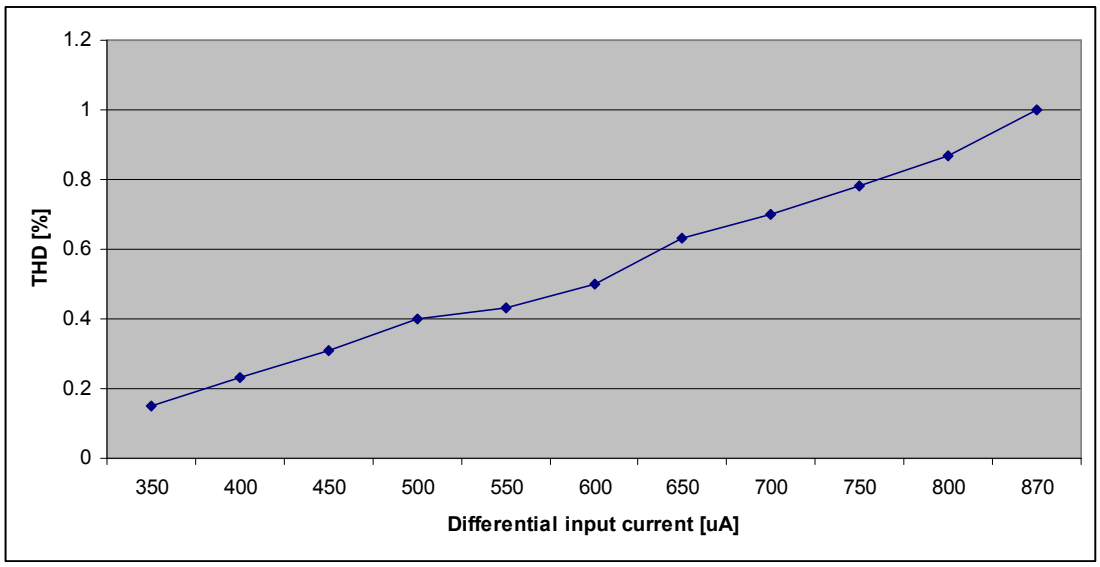


Figure 5.11 Simulated THD versus the differential input current of the current-mode fifth-order linear phase filter

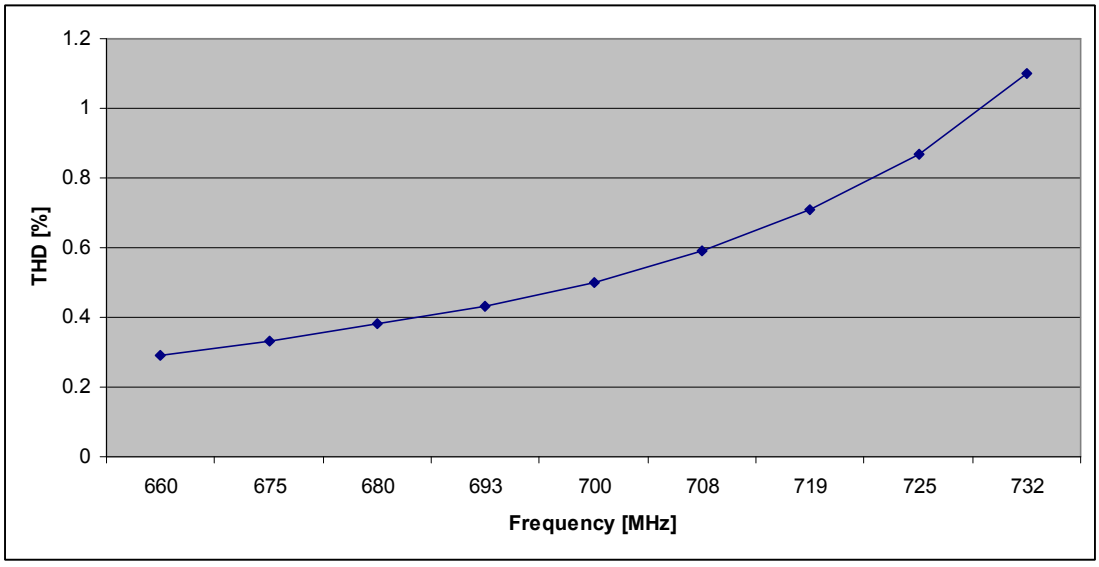


Figure 5.12 Simulated THD versus frequency of the current-mode fifth-order linear phase filter

Simulation of the filter has shown that the cut-off frequency of the filter without gain-boost can be tuned from 410MHz to 770 MHz with 90mW and 240mW, respectively. Moreover, the cut-off frequency of 720MHz is achieved with 190mW of

power consumption. The total RMS output noise current integrated over the bandwidth is 1.1uA$_{RMS}$. The DR is about 58dB at f_c=720MHz for the 1% THD.

5.4.3. Simulation Results of Voltage-mode Fifth-order 0.05° Equiripple Linear Phase LF Lowpass OTA-C Filter

Figure 5.13 shows that the magnitude responses of proposed voltage-mode filter using ideal VCCS and OTA in Figure 5.1.

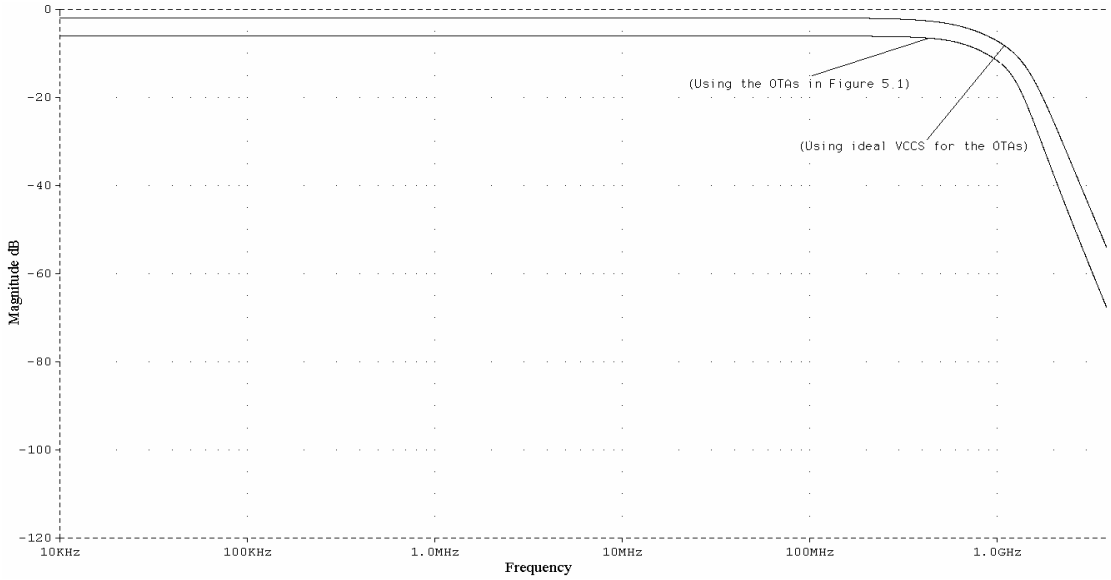


Figure 5.13 Simulated magnitude frequency responses of the voltage-mode LF fifth-order 0.05° equiripple linear phase lowpass OTA-C filter

The filter phase responses using ideal VCCS and OTA in Figure 5.1 are shown in Figure 5.14. The filter's group delay ripple for $0 \leq f \leq 2fc$ is approximately 4% with the group delay below ±30ps over the whole tuning range. As mentioned in Section 5.4.2, the finite DC gain of the OTAs also affects the group delay ripple of the voltage-mode filter. However, the group delay ripples with and without gain boost are still less than 5%.

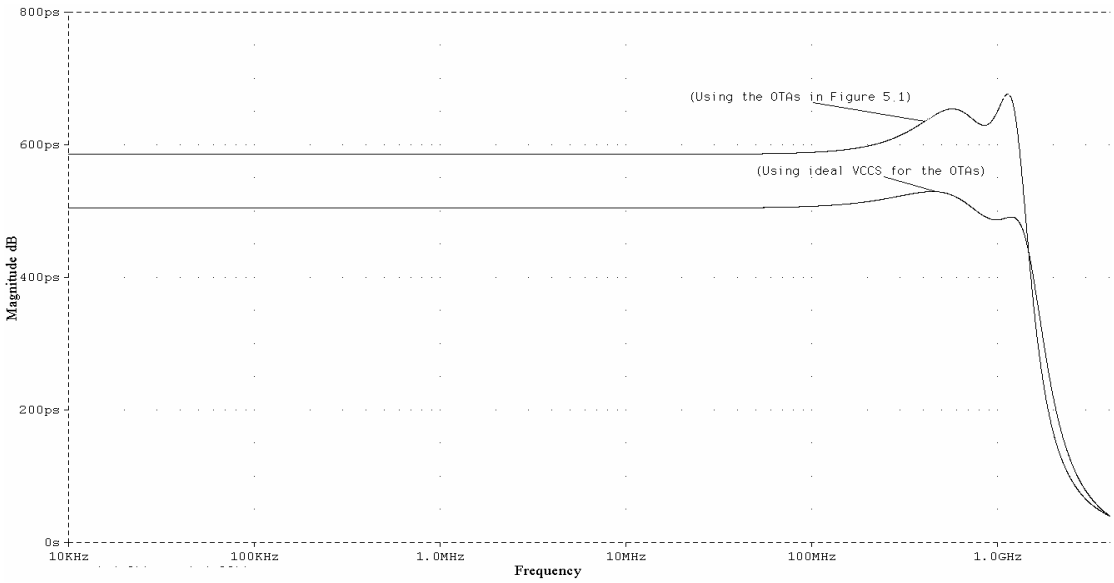


Figure 5.14 Simulated group delay responses of the voltage-mode LF fifth-order 0.05° equiripple linear phase OTA-C lowpass filter

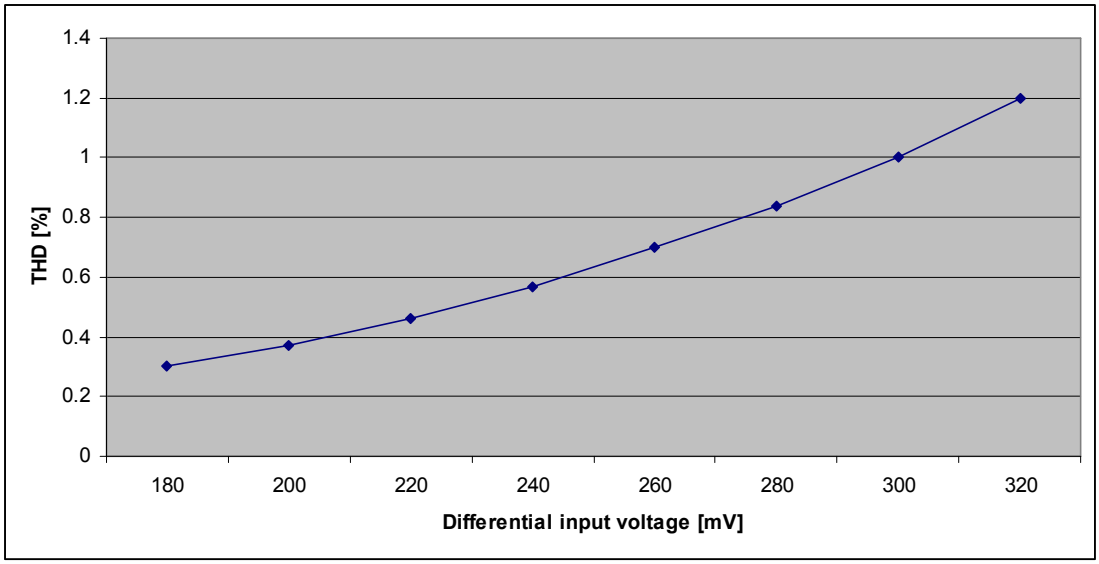


Figure 5.15 Simulated THD versus the differential input voltage of the voltage-mode fifth-order linear phase filter

The simulated THD as function of differential input voltage and frequency of the proposed voltage-mode filter are shown in Figures 5.15, 5.16, respectively. The simulated THD is less than 1% at differential input voltage up to 300mV. It also remains less than 1% for the frequency up to 750MHz.

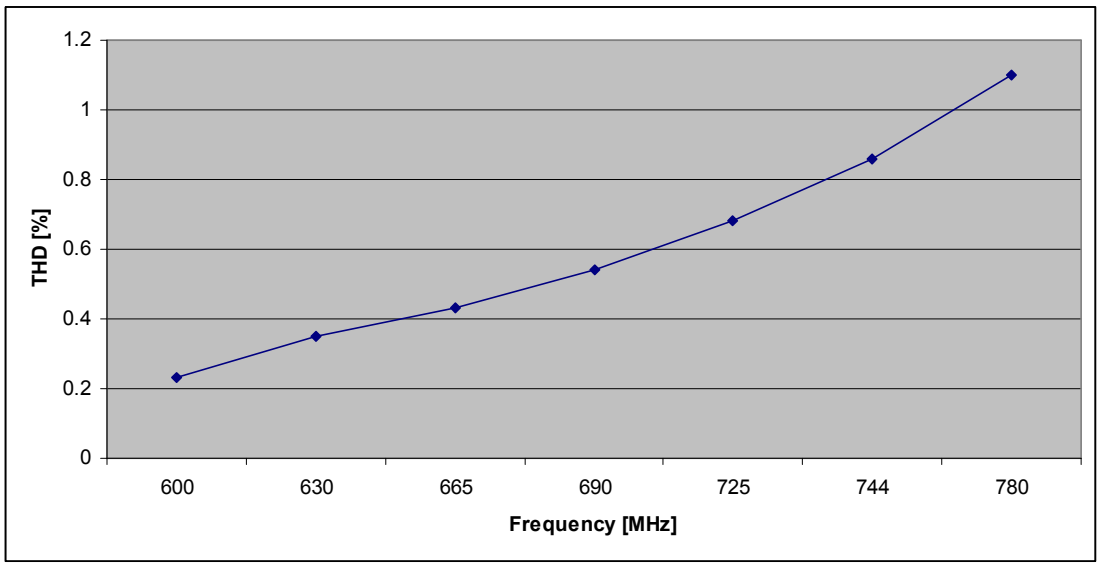


Figure 5.16 Simulated THD versus frequency of the voltage-mode fifth-order linear phase filter

The highest output voltage noise density appears at a level of about 2.6nV$_{RMS}$/√Hz. Approximation integration of noise over a bandwidth of 700MHz of the noise densities is about 70uV$_{RMS}$. Simulation also shows DR is about 51dB at *fc* =700MHz. The cut-off frequency of the voltage-mode filter without gain-boost can be tuned from 455MHz to 800 MHz with the same power consumption as their current-mode counterpart 90mW and 240mW, respectively. The 750MHz cut-off frequency is achieved with 190mW power consumption.

Comparing the presented filters with others in the literature, the performances of the filters offer significant improvements; especially the power consumption is much smaller than other designs, making the filter well suitable for portable electronics products. To compare the proposed solution with previous publications, the Figure of Merit (FOM) is defined in equation (5.28); all of the parameters such as bandwidth in MHz, geometry in μm, gain boost (GB) coefficient 1.5, and power consumption per pole in mW are taken into account.

$$FOM = \frac{GB \cdot [Bandwidth]^2 \cdot Geometry}{Power \ \ per \ \ pole} \tag{5.28}$$

The proposed filter has 3164 of FOM, which is much higher than any other MLF structures based filters in the literature. A comparison of the linear phase LF lowpass OTA-C filters designed and simulated in this chapter with other published in the literature is presented in Table 5.1.

Table 5.1 Performance comparison with different filter designs

Filter type	Filter configuration	Tech	*fc* range	GB	DR	FOM	GD
CM LF (This work)	5^{th} order 0.05° equiripple linear phase	TSMC 0.18µm	410-770MHz	6dB	58dB	3164	4% up to 1.7*fc*
CM FLF [59]	7^{th} order 0.05° equiripple linear phase	TSMC 0.18µm	55-160MHz	9dB	45dB	2430	5% up to *fc*
CM FLF [chapter 3]	7^{th} order 0.05° equiripple linear phase	TSMC 0.18µm	290-430MHz	8dB	54dB	3927	6% up to *fc*
CM LF [56]	7^{th} order 0.05° equiripple linear phase	TSMC 0.18µm	260-320MHz	5dB	66dB	810	4.5% up to 1.5*fc*
VM LF [36]	7^{th} order 0.05° equiripple linear phase	TSMC 0.25µm	8-32MHz	3dB	55dB	8.5	7% up to 1.1*fc*
VM LF [37]	7^{th} order 0.05° equiripple linear phase	TSMC 0.25µm	50-150MHz	6dB	65dB	272	5% up to 1.5*fc*
VM Cascade [41]	4^{th} order 0.05° equiripple linear phase	TSMC 0.35µm	550MHz	N/A	40dB SNR	3025	10% up to 1.7*fc*
VM Cascade [49]	5^{th} order Butterworth	TSMC 0.18µm	330MHz	24dB	40dB	3324	20% up to *fc*

VM Cascade [50]	4th order 0.05° equiripple linear phase	TSMC 0.35µm	80-200MHz	N/A	52dB	770	4% up to 1.4*fc*
VM Cascade [35]	4th order 0.05° equiripple linear phase	TSMC 0.5µm	100MHz	N/A	45dB	455	3% up to *fc*
VM Cascade [39]	7th order 0.05° equiripple linear phase	TSMC 0.35µm	160-220MHz	N/A	50dB	1628	4% up to 2*fc*
VM LC ladder [52]	7th order 0.05° equiripple linear phase	TSMC 0.25µm	80-200MHz	13dB	43dB THD	361	5% up to 1.5*fc*
VM Cascade [33]	8th order 0.05° equiripple linear phase	TSMC 0.25µm	30-120MHz	6-14dB	45dB	250	5% up to 1.5*fc*

5.5 Conclusions

The designed equalizers are CMOS current- and voltage-mode 750MHz fifth-order 0.05^{o} equiripple linear phase lowpass LF OTA-C filter with gain boost. The equalizers have been synthesized using the proposed iterative approach. To meet the current stringent requirements for read/write channel equalizer design, the use of a CMOS OTA with UHF capability, lower-voltage/lower-power operation, sufficient transconductance tuning range (to meet the relatively wider programmable gain boost), and lower excess phase (important for reducing filter group delay ripple) is also described. The equalizer utilizes the CMOS OTA was presented whose simulation results based on a standard TSMC 0.18µm CMOS process, standard simulation results were obtained for the equalizers with only manual fine adjustments (without on-chip tuning) of transconductances and pre-distortion of circuit capacitor values. In particular, reasonable group delay ripple (the key design specification) has been achieved, although it was previously reported that MLF based OTA-C filters suffer relatively large group delay errors [42, 43, 53, and 61]. Furthermore, the equaliser has

the lowest power consumption compared with previous designs as a result of relatively large transconductance value used in the design. Thus, CMOS current- and voltage-mode fifth-order LF 0.05° equiripple linear phase lowpass OTA-C filters can be expected to be suitable for next generation read/write channels with fully-balanced implementation and inclusion of a practical automatic tuning circuit.

6. Analogue Baseband Filter Design Considerations for Highly Integrated Multi-standard Receivers

6.1 Introduction

The growing economic and social impact of mobile telecommunication devices with the evolution of protocols and interoperability requirements among different communication standards for voice and data is currently driving worldwide research towards the implementation of fully-integrated, multi-standard receivers. Moreover, there is also a great demand for lighter and smaller communication devices with longer battery lifetime; hence compact, low voltage and low power consumption IC design solutions must be developed. This is particularly true as mobile, wireless communication is integrated in communication systems [3, 64, 66, 70-75]. Therefore, miniaturization without any degradation of performance is demanded for these multi-standard terminals. These new terminals should support both horizontal handovers, i.e., switching between different modes of the same system, and vertical handovers, i.e., switching between different systems, in the most compact, efficient and economical way. Therefore, a high degree of flexibility not only in the digital baseband and RF front-end but also in the analogue baseband is needed. Furthermore, the terminal should adapt itself to the changing channel conditions and user requirements to provide the required quality of service with the minimum power consumption. Traditionally multi-standard terminals have used a separate radio channel for each of the standards supported. This becomes increasingly unfeasible as the terminal becomes more diversified. A new model, therefore, emerges based on maximum hardware reuse from end to end coupled with a full CMOS implementation with the ultimate goal of a single chip solution. It is found; the direct conversion architecture is well suited for these terminals, because it does not need IF SAW channel-select filters and subsequent down-conversion stages, since the channel select function is achieved using lowpass filters and baseband amplifiers that are amenable

to monolithic integration. Therefore, direct down-conversion architectures have been attracting world-wide attention in recent years. With direct down-conversion architectures, several standards such as Bluetooth, GSM, WCDMA, WLANs, can be accommodated using a single receiver. This has obvious advantages in terms of reduction in power consumption and silicon area. The intermediate frequency filtering requirement is changed from bandpass filtering to lowpass filtering in the direct conversion receiver. Although there are a number of high-performance bandpass filter designs in the literature [65, 67, and 99], it is still a major challenge to achieve high Q and guarantee the accuracy of filter tuning [68]. Moreover, the intermediate frequency may significantly vary depending on the different systems. Therefore, the direct conversion architecture is easier to integrate in standard semiconductor technologies. Implementation of an integrated multi-standard receiver that is competitive with solutions based on separate devices for the different standards must take various points into account. First of all, both silicon area and static power consumption must be minimized, thus requiring the maximum possible hardware sharing among the receivers for the different standards. Based on these considerations, multi-standard receiver architecture can be defined, as shown in Figure 6.1 [70, 72, 75-83, 93].

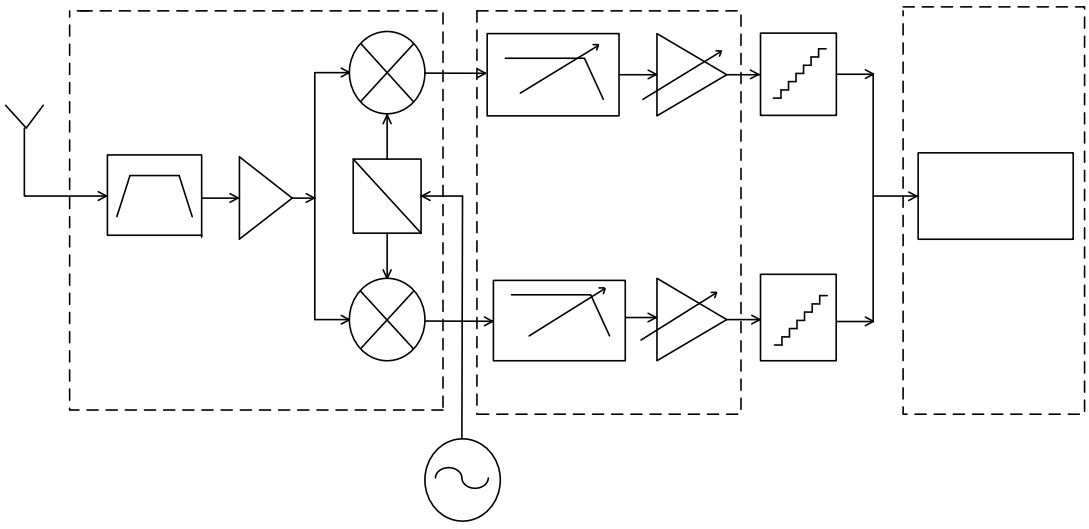


Figure 6.1 Receiver channels

After the RF signal is selected by the external RF filter and amplified by the LNA, the signal is mixed directly to DC by a quadrature mixer. The analogue baseband filter performs the channel selection before A/D conversion. The analogue baseband block of the receiver is composed of variable gain amplifiers (VGA) and lowpass filters. The VGAs increase the signal amplitude, while the lowpass filter reduces the amount of the out-of-band signal in order to increase the dynamic range available for the useful signal. The design of the receiver baseband channel implies a trade-off between lowpass filter selectivity and circuit complexity. The higher filter selectivity would result in a lower number of stages.

The key building blocks for a complete RF front-end for personal communication system applications have been demonstrated in CMOS [69, 70]. The baseband digital circuitry is currently implemented in standard sub-micron CMOS, therefore there is a tendency to use the same digital CMOS processes for baseband data converters and analogue filters. Traditionally in CMOS, baseband filters are realized using switched-capacitor (SC) techniques. However, biasing MOS switches fully on or off and maintaining proper operational amplifier (Op-amp) operation is difficult to achieve in SC circuits with reduced supply voltage. Moreover, the SC filter needs a sampling frequency that is much higher than the cut-off frequency. This requires the use of op-amps with very wide bandwidths, demanding large bias currents. Therefore, in high-speed analogue systems such as HDD applications and systems such as CDMA with signal bandwidths over several hundreds of kilohertz, continuous-time active-RC, and OTA-C filter structures tend to be implemented. OTA-C filters have the advantages that they do not require extra processing steps compared to active-RC filters, and their frequency tuning is easily achieved by using dc bias currents, but they have poor linearity and automatic on-chip tuning circuits are needed. On the other hand, the active-RC filter has a very good linearity characteristic, but high power consumption and large chip area compared with OTA-C type filters due to having integrated resistors; it is also more difficult to achieve very high cut-off frequency using active-RC filters. Therefore, the trade-offs between active-RC and

OTA-C filters must be considered carefully and the overall system design is affected by choice of filter structures.

This Chapter focuses on the design issues of different types of filter for multi-standard receivers. The Chapter is organized into seven Sections. Design challenges of receiver analogue baseband and channel select filters are addressed in Section 6.2. The Section 6.3 and Section 6.4 discuss active-RC and OTA-C filters for multi-standard applications, respectively. In Section 6.5, a fourth-order OTA-C baseband filter for Bluetooth, WCDMA and WLAN is designed using MLF LF configuration. Future directions of multi-standard filter design are given in Section 6.6 and conclusions are shown in Section 6.7.

6.2 Receiver Analogue Baseband and Channel Selection Filters

The signal spectrum at the input of the receiver baseband block includes unwanted components such as in-band and out-of-band blockers, and adjacent channel signals which can dominate the signal to be processed. For this reason analogue baseband blocks are required to exhibit not only a target in-band dynamic range, but also excellent linearity for out-of-band signals. This is because non-linear behavior with out-of-band signals would result in intermodulation products falling within the signal band, corrupting the signal. An important function of the analogue baseband circuitry is channel selection and anti-alias filtering of signals from the I/Q down-converter. Therefore, in multi-standard receivers, the analogue baseband circuit must handle a range of signal bandwidths. The baseband signal bandwidths vary, for example, from 500 kHz for the Bluetooth to 12 MHz for an 802.11b receiver. A summary of different standards is given in Table 6.1. Moreover, the specifications of different systems vary, which may result in different requirements for in-band and out-of-band attenuation. Both of digital and analogue filters can be used to achieve the channel selection functions. From the channel selection point of view, the digital channel selection filter is well suited to multi-standard applications, because of the ease of

changing the specifications of the filter [71]. However, the linearity and resolution requirements of the analogue to digital converter (ADC) are then critical; due to the wide dynamic range of signals at the ADC input. The ADC must be able to accommodate the received signal and high level blocking signals simultaneously. Therefore, $\triangle\Sigma$-modulators are typically used with digital channel selection schemes for ADC design. However, analogue baseband filtering has attracted more attention than digital filtering due to power efficiency issues. In particular, for systems with a wide channel bandwidth, relying on a high-resolution ADC tends to be power hungry.

Table 6.1 Wireless communication systems

Standard	GSM	Bluetooth	WCDMA CDMA2000	802.15/ZigBee	802.11/ WLAN	802.16 WiMax	UWB
Application	Voice	Voice/ Data	Voice/ Data	Data	Data	Data	Data
Bandwidth	200kHz	500 kHz	2.11-5 MHz	2.5MHz	10-12 MHz	30MHz	250MHz
Modulation	GMSK	GFSK	QPSK	QPSK	OFDM	OFDM	OFDM

Therefore, in many applications, it is more economical to implement an analogue filter and variable gain amplifier (VGA) to realize channel selection functions with an ADC requiring a reasonable dynamic range. However, design of the analogue baseband section of reconfigurable receiver is a complex task. It requires optimization of bandwidth, linearity, power consumption, silicon area, and noise [72]. Theoretically, one could design a filter optimized for the most stringent requirement of each standard. However, this approach is normally not efficient in terms of power consumption and silicon area. There are a number of compromise approaches which have been described in the literature; some examples are reported in the following

sections.

The most important function of a multi-standard analogue baseband filter is to control the cut-off frequencies over the required range of bandwidths. A number of alternative continuous-time filter techniques have been proposed, such as active-RC, OTA-C, and SC. Among these different techniques active-RC and OTA-C techniques have been widely used. In continuous-time analogue filters, the cut-off frequencies can be tuned by changing bias voltages or currents; in order to realize multi-standard functionality. However, some specifications, such as power consumption, noise, and especially linearity are also changed when varying bias voltage or current. The tuning principle is depicted in Figure 6.2. As can be seen, the cut-off frequency control is often implemented in switched-standards rather than by simply extending the tuning range.

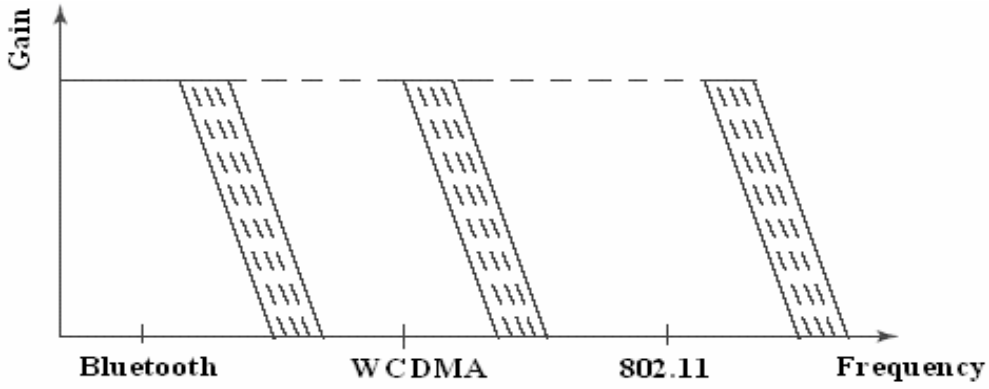
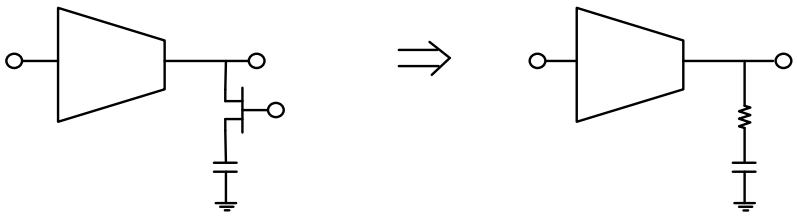


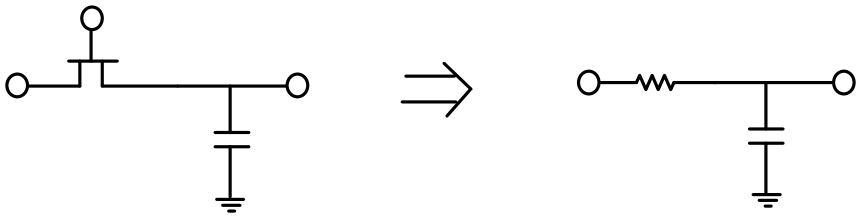
Figure 6.2 Filter cut-off frequency: standards switching

The cut-off frequency of an active-RC filter is changed by tuning either the capacitors or resistors, or both. In the OTA-C filter case, tuning of the transconductance or capacitors can be used. The discussion in this section is mostly focused on these two filter techniques for multi-standard applications. As mentioned, the digital controlled switches have to be used, which can be implemented as triode region MOSFET. As can be seen from Figure 6.3, once the MOSFET is on, it acts like a resistor due to the limited on-resistance R_{on}. Therefore, adding switches in series with integrating capacitors causes a phase lead in the integrators, while adding

switches to the signal path, whether at the input or output of the integrators, causes a phase lag. As a result the filter frequency response becomes poorly controlled.



(a)



(b)

Figure 6.3 (a) Adding switch in series with capacitor, (b) Adding switch to the signal path

Therefore, it is needed in switch design to minimize these effects. Although the effects on the filter cut-off frequency are ideally the same, the noise produced by the filter is affected in different ways, by the tuning approach which is chosen. If the resistance or transconductance is changed to perform cut-off frequency tuning, the integrated thermal noise of the filter will remain roughly the same. However, the noise voltage density will be inversely proportional to the cut-off frequency making the spot noise figure of the baseband filter dependent on the mode. Moreover, transconductance tuning normally achieved by changing dc bias or gate voltage of triode region transistors, both of them is strongly related with power consumption and linearity. Alternatively, if only the capacitor values are tuned, the noise voltage density and spot noise figure remain approximately constant, while the integrated noise voltage is directly proportional to the cut-off frequency. The capacitors in

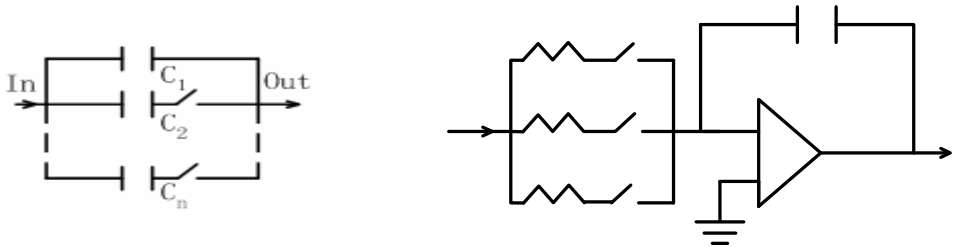
Input

V cont

particular tend to dominate the filter silicon area for narrowband systems; therefore, a pure capacitor-tuning approach may not be viable, depending on the capacitance density of the technology [73, 74]. Therefore, the design of analogue multi-standard filters involve complex trade-offs between power consumption, silicon area, linearity, and speed.

6.3 Multi-standard Active-RC Filters

Most proposed active-RC filters use capacitor arrays, resistors array or a combination of these two methods to control the cut-off frequency [73, 75, and 76]. The tuning techniques are shown in Figure 6.4.



(a) (b)

Figure 6.4 (a) Capacitance matrix, (b) Active-RC integrator with band switching resistors

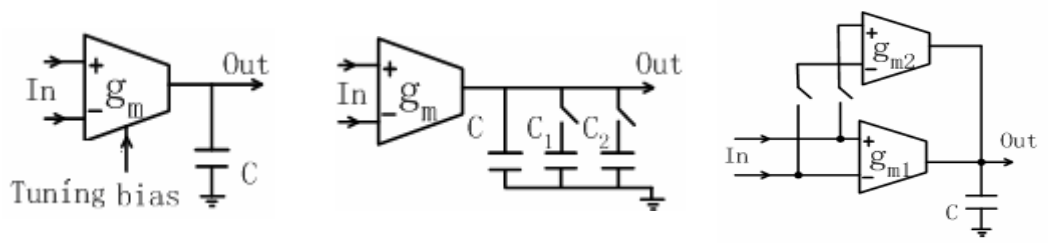
The capacitance and resistance values can be changed by switching on and off switches at each branch. In principle, either switching approach can be used to achieve the same tuning range. However, constant-capacitance scaling keeps the dynamic range constant, irrespective of the bandwidth. Hence, no over-design is needed, which means the less power consumption and smaller chip area is guaranteed. If the original filter is designed optimally in terms of white noise and distortion, then any constant-capacitance scaled version of it will also be optimal, irrespective of its bandwidth. In addition, constant-capacitance scaling can result in a design technique that is remarkably immune to effects of parasitic capacitances; for example, in [87, 88]. In [82], the integrator capacitors, which were disconnected in a wideband mode (WCDMA), were reused in a DC-offset cancellation loop to offset the area cost. The

main drawback of both switching methods is the difficulty of avoiding parasitic effects due to CMOS switches in the signal path. With switched integration capacitors, the phase lead introduced by the switched on resistance tends to compensate for the finite Op-amp unity gain bandwidth product (GBW) and this effect may even be utilized to save power if the switch resistance is properly controlled. With resistors, a major concern is non-linear effects due to the switch, which has led to the practice of connecting the switches to the Op-amp input. If larger switches are used to achieve better linearity, this has the effect of adding capacitance to op-amp input and degrading the phase margin of the op-amp. Reconfigurable active blocks can be used to minimize analogue baseband power consumption, when reduced signal bandwidth is selected. Theoretically, the power consumption of an op-amp is reduced in proportion to its required GBW which is smaller for narrower bandwidths. The easiest way to accomplish GBW control is to simply change the bias current of operational amplifier [75, 81]. However, linearity and phase margins can be better optimized for different operating modes if input and output stage transistor dimensions are also changed [72]. Other techniques, such as the grounded amplifier and fully balanced differential difference amplifier (FBDDA) are also found in the literature [89]. References [83, 85] designed channel selection filters using a compensated one-pole Op-amp, similar to [84].A multi-standard baseband filter reported in [90] realizes integrators as a combination of current and voltage buffers. It achieves a very wide tuning range by using an R-2R network in place of input resistors, and digitally controlled current divider networks inside the current buffers which yield a total of 14 bits resolution for the frequency control. The performance of this filter is comparable to active-RC based filters. However, the internal current divider network in the current buffer makes it difficult to adjust the current consumption of filter, depending on the filter cut-off frequency.

6.4 Multi-standard OTA-C Filters

The OTA-C technique offers the advantage that the transconductance can be tuned

continuously, as shown in Figure 6.5(a).



(a) (b) (c)

Figure 6.5 (a) Gm tuning, (b) Tuning using switched capacitance, (c) Tuning using switched OTAs

This is accomplished either by controlling the bias current of the input transistors, or their drain-source voltage in the case of triode-region MOS transconductors. A transconductor design with a very wide tuning range is needed to realize the required cut-off frequency tuning range. Such an approach has been adopted in [92] for implementing a filter with a cut-off frequency tunable from 0.5 MHz to 12 MHz. The main limitation of using the transconductance control only is that the linearity of the transconductor is dependent on the tuning bias; normally, the larger bias current that is used, the better the linearity that is achieved. Moreover, the linearity is not constant. In [33, 91], the transconductance-control-only circuit makes it difficult to meet linearity requirements for filter cut-off frequencies close to the minimum while achieving high power efficiency for cut-off frequencies close to the maximum. Transconductance tuning can be combined with switched tuning for selecting the operating standard, which greatly relaxes the required transconductance tuning range. Either the capacitors, as shown in Figure 6.5(b) [93], or the transconductors, as depicted in Figure 6.5(c) [93, 94] can be switched to make a large step in the cut-off frequency. Analogue circuits based on the operational transconductance amplifier (OTA) and capacitor (OTA-C) technique is promising for high-frequency operation [41]. Having an OTA of programmable transconductance and a programmable capacitor, it is possible to design filters for a wide frequency tuning range. For most CMOS processes, it is not possible to create a capacitor with a wide range of

programmability which can operate at high frequencies. Therefore, the transconductor must have a wide tuning range. The proposed OTA in [95] has transconductance that can be adjusted by a factor of 700. This results in the possibility of designing filters with cut-off frequencies from several kilohertz to several megahertz. The OTA-C technique is considered to offer such advantages as high speed and low power [87, 92, and 41] but also has limited applicability because of low dynamic range and poor linearity compared with the active-RC technique [86]. In order to increase the dynamic range of OTA-C filters, transistor level design is most important, because the linearity of the filter is directly related to the linearity of the OTA. Therefore, a wide range of techniques have been proposed in literature to improve the linearity of transconductors. Using current conveyors [96] and resistors as building blocks, it is possible to design highly linear transconductors, thus extending the usefulness of the technique to applications requiring high linearity. There is a trade-off between linearity and power consumption. Source degeneration OTA circuit topologies are widely used in HDD applications in order to optimize the linearity and power consumption. In [94, 97], low power consumption and large dynamic range is achieved. The drawback is relatively small tuning range. To avoid this problem, a so-called negative source degeneration resistor (NSDR) OTA circuit topology is proposed in [92]. In addition, a new adaptive DC-blocking, triode-biased MOSFET (ADTM) transconductor is proposed in [91], which enables wide and continuous frequency tuning with low power consumption. A single OTA integrator-based OTA-C filter may be needed to further reduce power consumption and chip area [98].

The OTA-C technique is vulnerable to all parasitic components; this includes the effect of switches in series with capacitors or elsewhere in the signal path. The filter circuit structure plays an important role in determination of filter performance. The cascade structure can be implemented with lower power consumption and smaller silicon area than ladder simulation methods, but sensitivity is relatively high. On the other hand, ladder simulation structures have low sensitivity, but cost more power consumption and chip area due to the need for extra OTA convert floating capacitors

to grounded ones. It has been proved that the MLF structure has lower sensitivity than the cascade and less complexity than ladder simulations. Recently, multiple loop feedback (MLF) structures have been used for HDD applications [36, 37, 55-59]. They achieve good performance at very high frequency with reduced parasitic effects and simple design methodologies. Therefore, the MLF filters are potentially suitable for multi-standard analogue baseband filter design. However, use of this type of structure has not been found in the literature.

6.5 Design and Simulation of MLF OTA-C Filter for Multi-standards

Although the cascade and LC ladder simulation methods have been used for multi-standards analogue baseband filtering design [69-83, 85-87, 90-99, 102, 103], the MLF method has not been used for this application. Therefore, a fourth-order current-mode Butterworth lowpass filter based on the MLF LF configuration is proposed as an example in this section, with cut-off frequency can be tuned from 500 KHz to 12MHz to cover Bluetooth, WCDMA and WLAN.

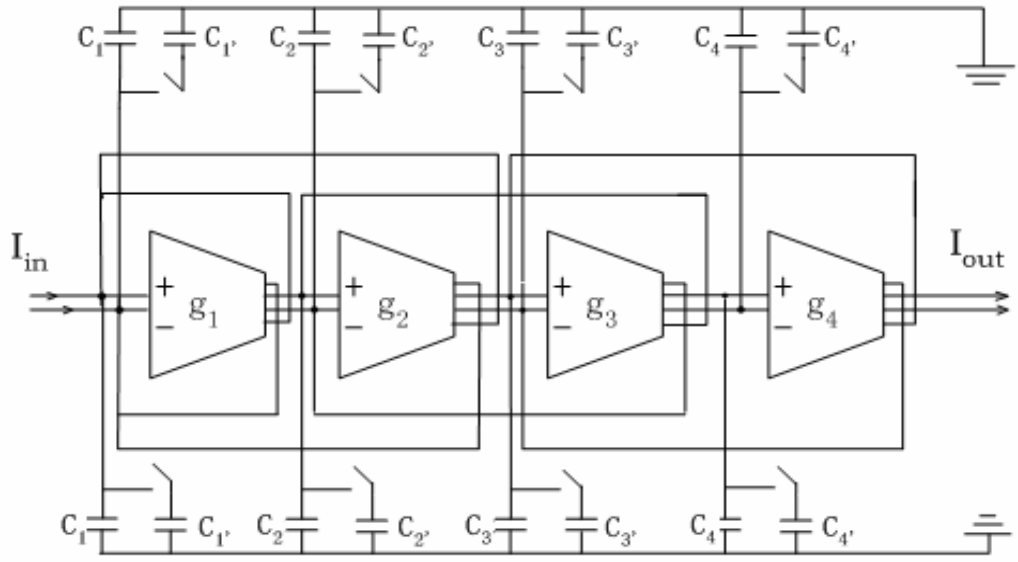


Figure 6.6 Fourth-order current-mode Butterworth LF OTA-C lowpass filter

The OTA-C implementation of the filter is shown in Figure 6.6. The structure with all

switches off, that is, with C_j is for WLANs, while when all switches are closed, or with C_j+C_j', it is for Bluetooth and WCDMA.

The normalized characteristic of a fourth-order lowpass Butterworth filter is given by:

$$H_d(s) = \frac{1}{s^4 + 2.61313\, s^3 + 3.41421\, s^2 + 2.61313\, s + 1} \tag{6.1}$$

The overall transfer function of the circuit has been derived as [Chapter 4]:

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{1}{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s + 1} \tag{6.2}$$

where the time constant $\tau_j = C_j/g_j$, C_j is the capacitance of capacitor j and g_j is the transcendence of OTA_j

The design formulae for the multi-standard filter can be attained by coefficient matching between (6.1) and (6.2). For n=4, the design formulae can be obtained as:

$$\tau_1 = \frac{B_4}{B_3}, \quad \tau_2 = \frac{B_3}{B_2 - B_1\tau_1}, \quad \tau_3 = \frac{B_2 - B_1\tau_1}{B_1 - \tau_2}, \quad \tau_4 = B_1 - \tau_2$$

Therefore the resulting pole parameters are:

$$\tau_1 = 0.3827\ , \tau_2 = 1.0824\ , \tau_3 = 1.5772\ , \tau_4 = 1.5307$$

Selecting identical transconductance g_m of 50μS and the cut-off frequency of the filter is chosen as 5MHz, using the computed τ_j values, the capacitor values can be calculated as:

$$C_1 = 1.22\ pF\ , C_2 = 3.45\ pF\ , C_3 = 5.02\ pF\ , C_4 = 4.87\ pF\ ,$$
$$C'_1 = 6.1\,pF\ , C'_2 = 17.23\ pF\ , C'_3 = 25.1\,pF\ , C'_4 = 24.37\ pF\ ,$$

MOSFET switches are used in the capacitor arrays of Figure 6.6, which is shown in Figure 6.7.

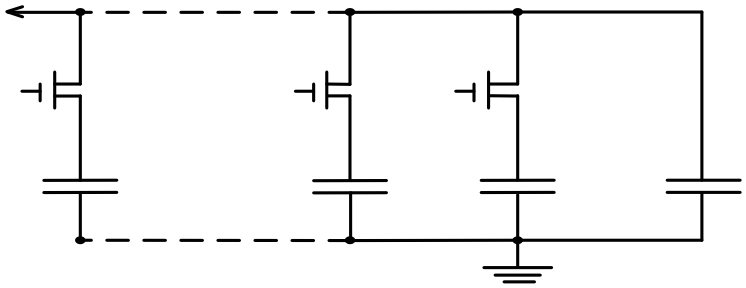


Figure 6.7 Switched capacitors array

The CMOS OTA in Figure 5.1 is used for the filter design. The circuit was designed and simulated using BSIM 3v3 Spice models for a 2.5V TSMC 0.18μm CMOS process available from MOSIS [112, 113]. In Figure 6.8, the simulated AC responses of the designed filter are plotted. The cut-off frequency of the filter can be tuned from 510 kHz to 11.2MHz.The power consumption of the filter is 9.8mW for Bluetooth and WCDMA applications, and 11.9mW for WLAN applications. The IIP3 is 21.8dBV for WLANs and 17.3dBV for Bluetooth and WCDMA. In the similar way, other MLF filters such as the FLF and IFLF [1-4, 59, 127] can be used for multi-standards analogue baseband applications.

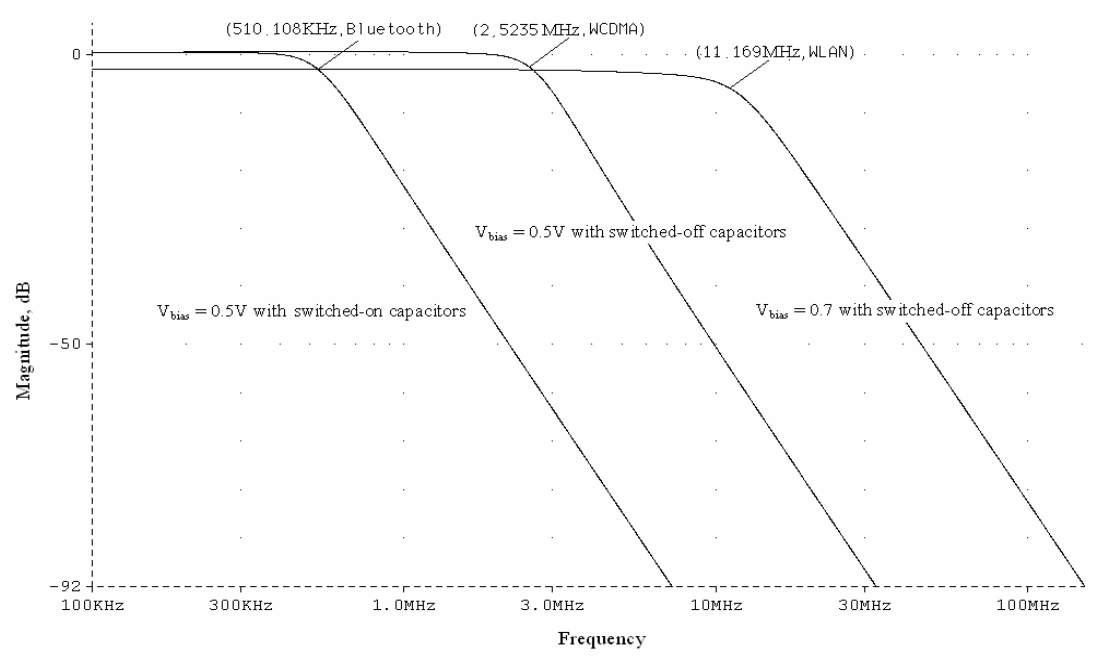


Figure 6.8 Simulated AC responses of proposed filter

6.6 Future Directions

The demand is driving the need for multi-radio platforms that include new licensed and unlicensed air interface technologies, such as ZigBee [99], WLAN, UWB, WiBro and WiMax. Furthermore, the applications like multi-band TV tuners are needed as well [100]. Finally, even more mobile TV standards are emerging worldwide, such as MediaFLO™ in the United States and DMB-T in China. Since mobile TV subsystems will be battery operated and will need to fit in the crowded cellular phone case, implementations that are small in size and consume low power are required. In addition, multi-standard capability is desirable since it will reduce cost for integrators and will allow users to receive mobile TV in their devices as they travel [101]. The information society is moving toward a merge between communication, computing and multimedia with the goal of a broad bandwidth connection for all at any time and any place. Within this framework, the 3G, 4G mobile telephone systems and various different kinds of wireless networks (for example WAN, WLAN and PAN) will be seamlessly interconnected to suit user needs. To operate in a smooth and transparent way between all these different wireless access systems on a common IP-based platform, new multi-standard multimode terminals are required. Research towards this goal aims to develop the key blocks of a reconfigurable terminal that supports many standards, such as Bluetooth, WCDMA, and WLAN, that are able to operate as nearly simultaneously as possible. The key characteristics of overall research are to achieve reconfigurability across the entire transceivers. The baseband bandwidths of Bluetooth, GSM, 3G and WLAN standards range from a few hundreds of kilohertz to a few tens of megahertz. With rapid developments, more and more standards and technologies will be used for future communications, such as WiMax, WiBro, and ultra wide band (UWB) [103]. All of these emerging standards have bandwidth requirements from a few tens megahertz to a couple of hundred megahertz. It is still a major challenge to implement an analogue baseband filter whose tuning range can be as large as 1:500 in order to cover all existing and future standards, although a tuning

range of 1:20 is currently possible.

6. 7 Conclusions

Design considerations for analogue baseband lowpass filters, for use in multi-standard receivers based on the direct conversion architecture, has been presented in this chapter. Design trade-offs in relation to power consumption, linearity, silicon area, and large tuning range have been discussed. In the literature, different filter architectures have been used to implement analogue baseband filters. Active-RC and OTA-C based filters are most popular [69, 94, and 99]. Although, active-RC structures exhibit excellent linearity at the cost of high power consumption, it is difficult for active-RC filters to achieve high cut-off frequencies, which means that active-RC filter structures are not very suitable for future wideband and mobile communications. On the other hand, OTA-C filters feature a reduced linear range but with low power consumption and small silicon area. Therefore, OTA-C filter structures will attract more attention in the near future, especially for wideband wireless applications due to their high frequency capability. The limited linearity can be further improved by integrated resistors or other OTA linearization techniques [102]. Moreover, although suitable lowpass filters can be implemented by BiCMOS, SiGe or a combination of these technologies, monolithic implementations using pure CMOS technology remains highly desirable for future communication systems design. A CMOS fourth-order current-mode Butterworth OTA-C lowpass filter was designed as an illustrative example. The simulation results well match the desired goals for operation with the Bluetooth, WCDMA and WLAN standards. With the convergence of communications, broadcasting and computing, future mobile terminal or handset must be highly programmable to accommodate any emerging standards. A high performance analogue filter system with a reconfigurable architecture and tunable parameters will thus be needed.

7. Design and Simulation of MLF OTA-C Filters for Wireless Communication Receivers

7.1 Introduction

As was discussed in last chapter, the continuous-time filter (CTF) is one of the most important building blocks in analogue domain. It plays a very important role in modern wireless communication systems. In receivers, very demanding high-performance analogue filters are typically used to block interferers and provide anti-alias filtering before the subsequent analogue to digital conversion stage. However, it is challenging to design analogue filters with low power consumption, high speed and large dynamic range [2-4].

There are three types of filter, which have been widely developed: switched-capacitor, active-RC, and OTA-C filters. Switched-capacitor filters are popular owing to excellent accuracy, but the switching noise and clock feed-through degrades the performance of the filter considerably in high frequency range. The signal bandwidth of next generation wireless communications such as WiMax, 802.11 exceed 30MHz. For this frequency range, OTA-C solutions are generally preferred due to the more efficient operation of wideband OTA. On the other hand, the performances of the OTA-C filter not only rely on the OTA, but also rely on the methodologies of filter design. There are three different methods to implement analogue filters: cascade, LC ladder simulation, and multiple loop feedback (MLF). The cascade method is not normally used for elliptic filter design due to high sensitivity. The LC ladder simulation method has been widely used for analogue elliptic filter design. However, as discussed in previous Chapter, LC ladder simulation approach requires some good knowledge of passive RLC filters and the active simulation process, whilst the MLF approach involves non-trivial matrix manipulation; although it has lower sensitivities compared with cascade method. On the other hand, LC ladder simulation approach needs to convert passive components into OTA and

connected high impedance nodes with floating capacitors. The main concerns are that the floating capacitors have higher sensitivity comparing with grounded ones. Moreover, the floating capacitors also occupy more die area. It has been proved that the MLF structure has lower sensitivity than the cascade and less complexity than LC ladder simulations. They achieve good performance at high frequency with reduced parasitic effects and simple design methodologies [4].

Although both Chebyshev and elliptic approximation have been realized for wireless communication applications in the literature, the order of the Chebyshev filter is always higher than the order of the corresponding elliptic filter. Thus the most economical filter will be the elliptic filter. However, MLF OTA-C based configurations have not so far been used for design of elliptic filters for wireless communications in the literature. Therefore, a number of fifth-order elliptic OTA-C lowpass filters for next generation wireless communication receivers are firstly presented in this Chapter, based on current-mode MLF FLF and LF configurations and voltage-mode IFLF and LF configurations. This Chapter is organized in the following way: The design of the OTA is discussed in Section 7.2. The filter synthesis and architecture is described in Section 7.3. The simulation results and conclusions are given in Section 7.4 and 7.5, respectively.

7.2 Transistor Level OTA Design

In general, the bandwidth of the OTA used in the filter must be much larger than the filter cut-off frequency. The OTA must also have with linearity in order to achieve acceptable low distortion levels. For high frequency filters, single stage OTAs are preferred, because the internal nodes of multi-stage designs result in additional excess phase shift, as well as increased power consumption. Source degeneration OTAs become popular due to their favourable trade-offs between linearity and power consumption. A large source degeneration factor increases the linearity of the OTA. However, it also reduces the overall transconductance. The CMOS OTA structure in Figure 5.1 was chosen for the filter design in this section to optimize the linearity and

power consumption. Detailed analysis of this OTA has been given in Chapter 5. The main noise sources of the presented OTA are shown in Figure 7.1.

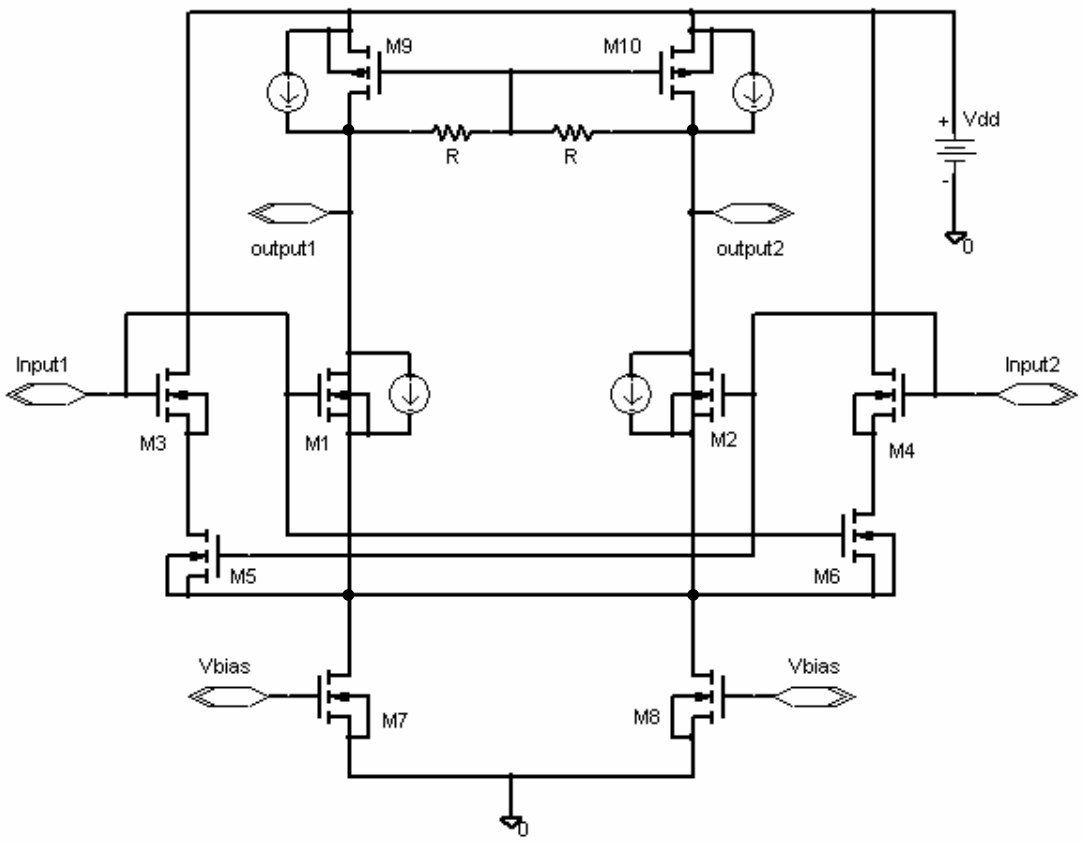


Figure 7.1 Noise source of the presented OTA

The transistors $M_{3\text{-}6,}$ are not in the output signal path, thus they have only common-mode noise. Similarly, the noise from M_7 and M_8 should give rise to negligible noise due to the fully balanced structure of the OTA. As a consequence, the main noise sources are from $M_{1,2}$, $M_{9,10}$, and the two resistors' R. For long-channel devices, the output noise of each cell can be readily expressed as,

$$V_n^2 = 2 \cdot \gamma \cdot [\frac{8}{3} K \cdot T \cdot B \cdot G_m \cdot R_{out}^2] \tag{7.1}$$

where K is the Boltzmann constant, T is the absolute temperature and B is the channel bandwidth. G_m is the small-signal transconductance of each input MOS transistors of the M_1, M_2 and R_{out} is the output impedance of OTA. The noise power is doubled because there are two branches. Note that the constant γ is 1 for long-channel devices

with noiseless loading. However, the output loading will introduce its own noise, and if short-channel effects, like the hot electron effect are taken into account, the value of γ can be up to four.

On the other hand, the output impedance of the single stage OTA is quite low, which leads to low dc gain. The limited dc gain will result in deviations of filter performance from the desired transfer function. An example is shown in Figure 7.2; the fifth-order elliptic filter using ideal VCCS and the OTA in Figure 5.1 is simulated. As can be seen, both passband ripple and stopband attenuation are out of the specifications.

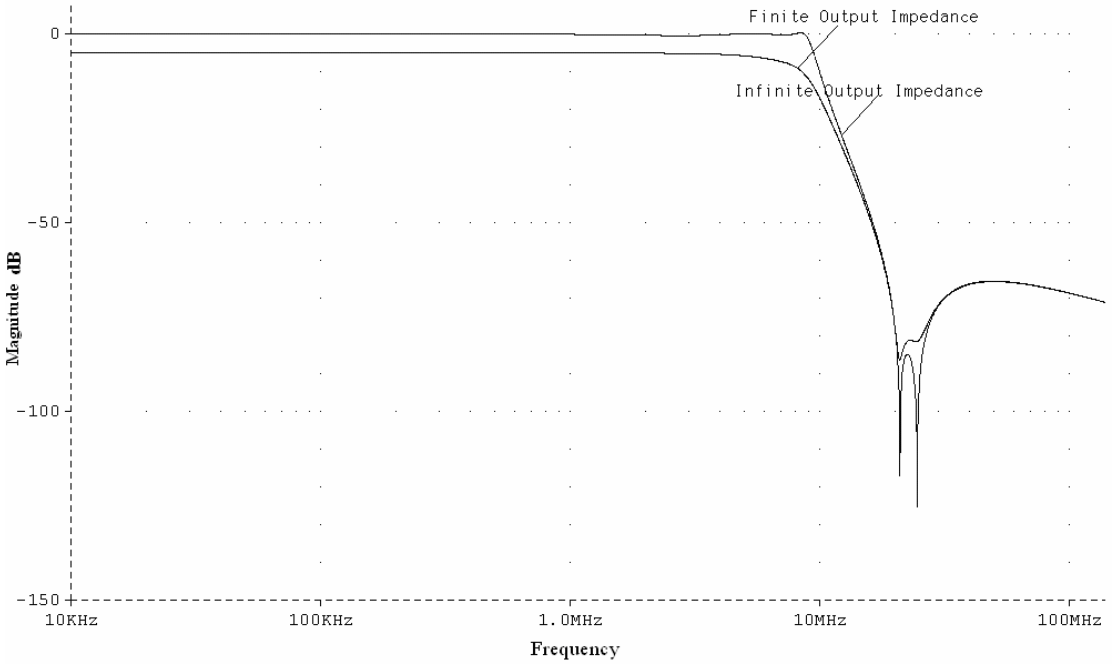


Figure 7.2 Comparison between the filter's ideal transfer function and the real one due to limited output impedance of OTA

The output impedance of the OTA must be therefore enhanced. This will move the low frequency pole as close as possible to dc, making it resemble an ideal integrator. One popular method to increase output impedance without introducing unwanted parasitic poles is to use a negative resistance load. This idea can be illustrated using the small signal model of an OTA shown in Figure 7.3.

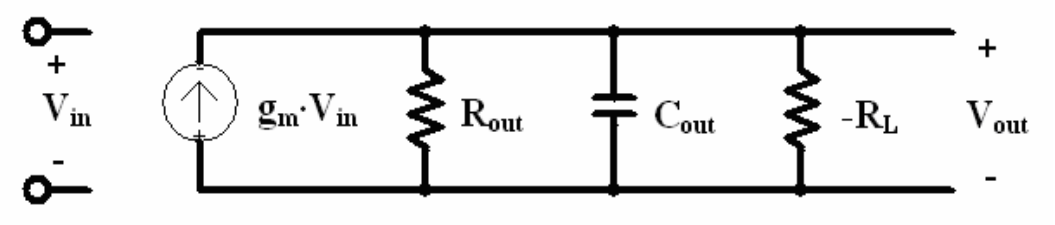


Figure 7.3 Small signal model of OTA with negative resistance load

The overall transfer function of Figure 7.3 is expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{g_m\left(\frac{R_{out}\cdot R_L}{R_{out}-R_L}\right)}{1+sC_{out}\left(\frac{R_{out}\cdot R_L}{R_{out}-R_L}\right)} \tag{7.2}$$

From equation (7.2), it can be seen that increasing the negative resistance $-R_L$ will result in increased DC gain, with DC gain reaching infinity when $R_L=R_{out}$. However, R_L must be less than R_{out} to ensure that the low frequency pole lies in the left half plane. To enhance the output impedance of the OTA, the negative resistance circuit can be implemented using an additional OTA, g_L, as shown in Figure 7.4.

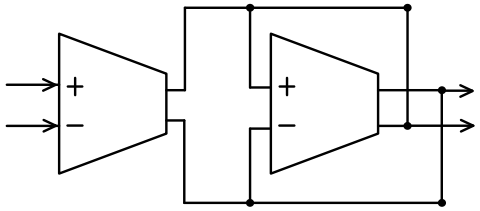


Figure 7.4 The diagram of simulated OTA with negative resistance

7.3 Filter Architecture and Synthesis

In this section, we present current-mode MLF FLF LF and voltage-mode MLF IFLF LF configurations implementing fifth-order elliptic OTA-C filters. In order to generally prove the availability of current- and voltage-mode MLF configurations for elliptic filters design, two different elliptic approximations for each mode are used.

7.3.1 Current-mode FLF Configuration

The circuit diagram of the presented current-mode fifth-order MLF FLF elliptic lowpass OTA-C filter is shown in Figure 7.5.

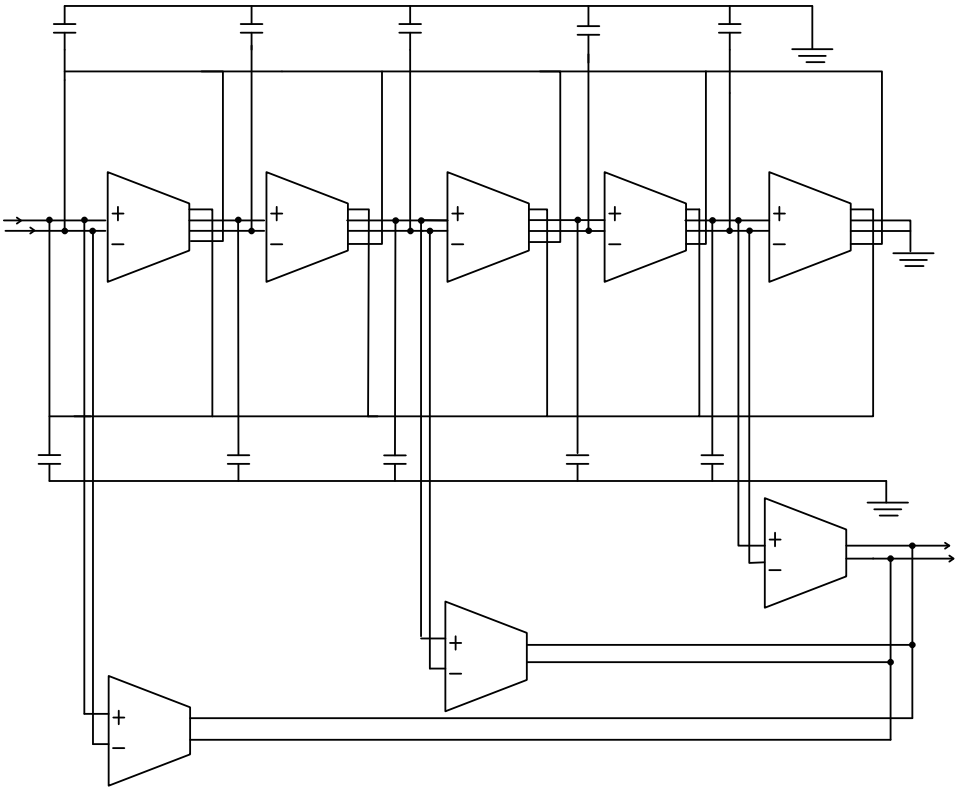


Figure 7.5 Current-mode fifth-order LF elliptic OTA-C lowpass filter

The general fifth-order elliptic lowpass transfer function can be written as:

$$H(s) = \frac{A_4 s^4 + A_2 s^2 + A_0}{B_5 s^5 + B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + 1} \tag{7.3}$$

Writing the current transfer function for the circuit in Figure 7.5 and comparing this function with equation (7.3), we can establish the following equations:

$$\tau_5 = B_1, \tau_4 = \frac{B_2}{B_1}, \tau_3 = \frac{B_3}{B_2}, \tau_2 = \frac{B_4}{B_3}, \tau_1 = \frac{B_5}{B_4} \tag{7.4}$$

$$\alpha_1 = \frac{A_4}{B_4}, \alpha_3 = \frac{A_2}{B_2}, \alpha_5 = A_0 \tag{7.5}$$

The normalized characteristic of a fifth-order elliptic OTA-C lowpass filter with

50dB stopband attenuation and 0.5dB passband ripple is given by:

$$H_d(s) = \frac{0.0758\,s^4 + 0.5962\,s^2 + 1}{3.949\,s^5 + 4.58\,s^4 + 7.953\,s^3 + 5.558\,s^2 + 3.501\,s + 1} \tag{7.6}$$

where time constants $\tau_j=C_j/g_j$ and zero parameters $\alpha_j=g_{\alpha j}/g_j$, therefore, for the current-mode fifth-order FLF elliptic OTA-C lowpass filter can be calculated as using equation (7.4) (7.5) and (7.6) [55, 106, 107]:

$$\tau_1 = 0.862\,,\ \tau_2 = 0.576\,,\ \tau_3 = 1.431\,,\ \tau_4 = 1.587\,,$$
$$\tau_5 = 3.5012\,,\ \alpha_1 = 0.02\,,\ \alpha_3 = 0.11,\ \alpha_5 = 1$$

The filter is designed with identical g_j using the CMOS OTA cell in Figure 7.1, with selected transconductance g_m of 4.5mS, to improve OTA matching and facilitate design automation. The cut-off frequency of the proposed filter is chosen as 30 MHz. Using the computed τ_j and α_j values, the capacitor values and $g_{\alpha j}$ values for the output summation OTAs can be calculated as:

$$C_1 = 41.16\,pF\,,\ C_2 = 27.5\,pF\,,\ C_3 = 68.33\,pF\,, C_4 = 75.77\,pF\,,$$
$$C_5 = 167.17\,pF\,,\ g_{a1} = 90\,\mu S, g_{a3} = 495\,\mu S,\ g_{a5} = 4.5\,mS$$

7.3.2 Current-mode LF Configuration

The circuit diagram of the current-mode fifth-order LF elliptic OTA-C lowpass filter is shown in Figure 7.6. The design formulae for the current-mode LF configuration is relatively complicated compare to those for the FLF configuration with FLF ones. There is not any iterative equation. The design formulae for current-mode fifth-order lowpass OTA-C filter are shown below [Chapter 4]. The transfer function for the current-mode fifth-order elliptic OTA-C lowpass filter in Figure 7.6 is given by:

$$H(s) = \frac{N(s)}{D(s)}$$

$$N(s) = \alpha_1\tau_2\tau_3\tau_4\tau_5 s^4 + [\alpha_1(\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5) + \alpha_3\tau_4\tau_5]s^2$$
$$+ (\alpha_1 + \alpha_3 + \alpha_5)$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3$$
$$+ (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1$$

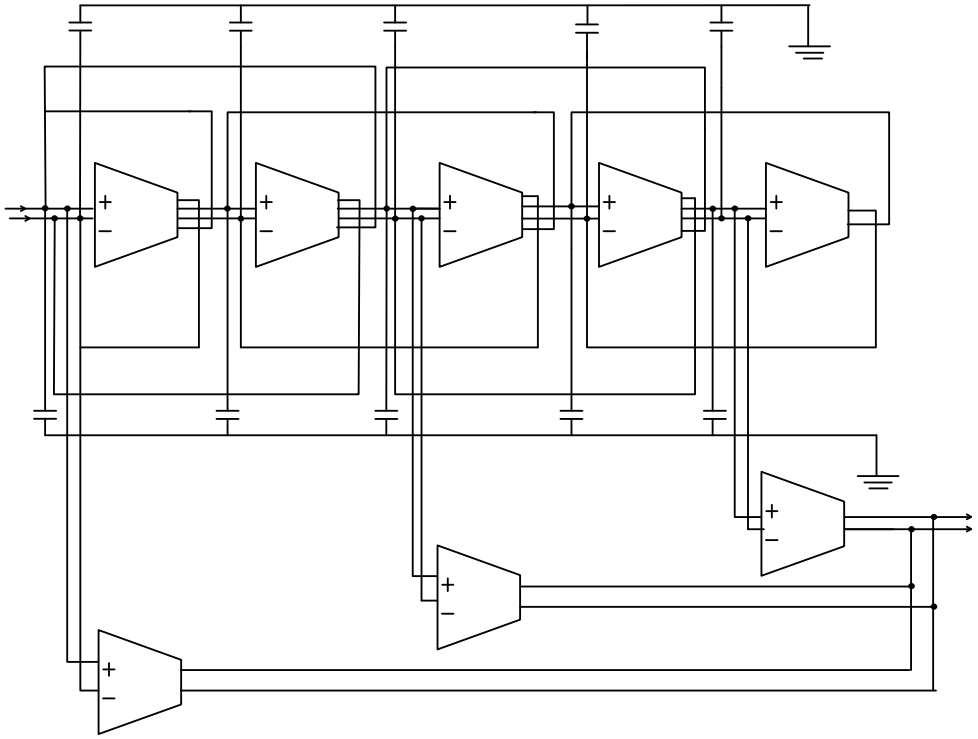


Figure 7.6 Current-mode fifth-order LF elliptic OTA-C lowpass filter

Then the time constant and zero parameters can be derived as:

$$\tau_1 = \frac{B_5}{B_4}, \tau_2 = \frac{B_4}{B_3 - B_2\tau_1}, \tau_3 = \frac{B_3 - B_2\tau_1}{B_2 - (B_1 - \tau_1)\tau_2}, \tau_4 = \frac{B_2 - (B_1 - \tau_1)\tau_2}{B_1 - \tau_1 - \tau_3},$$
$$\tau_5 = B_1 - \tau_1 - \tau_3, \tag{4.3}$$

$$\alpha_1 = A_4 / B_4, \alpha_3 = [A_2 - 2\alpha_1 B_2] / \tau_4\tau_5, \alpha_5 = A_0 - (\alpha_1 + \alpha_3)$$

(4.5)

Following the same procedure as for the current-mode FLF filter design and using another fifth-order elliptic approximation with 60dB stopband rejection and 1dB passband ripple, which is given by:

$$H_d(s) = \frac{0.0271\, s^4 + 0.324\, s^2 + 1}{4.692\, s^5 + 5.469\, s^4 + 9.263\, s^3 + 6.369\, s^2 + 3.839\, s + 1}$$

(7.7)

Using equation (7.7), (4.3) and (4.5), we can calculate:

$$\tau_1 = 0.858\ , \tau_2 = 1.44\ , \tau_3 = 1.829\ , \tau_4 = 1.802\ , \tau_5 = 1.152\ ,$$
$$\alpha_1 = 0.004\ , \alpha_3 = 0.132\ , \alpha_5 = 0.864$$

For the identical g_j (j=1 to 5) of 4.5mS, we can further calculate the capacitor and zero parameters:

$$C_1 = 41\ pF\ ,\ C_2 = 68.75\ pF\ ,\ C_3 = 87.19\ pF\ ,$$
$$C_4 = 86.01\ pF\ ,\ C_5 = 55\ pF\ ,\ g_{a1} = 18\ \mu S,$$
$$g_{a3} = 594\ \mu S,\ g_{a5} = 3.9\, mS$$

7.3.3 Voltage-mode IFLF Configuration

The voltage-mode fifth-order MLF IFLF elliptic lowpass filter is shown in Figure 7.7.

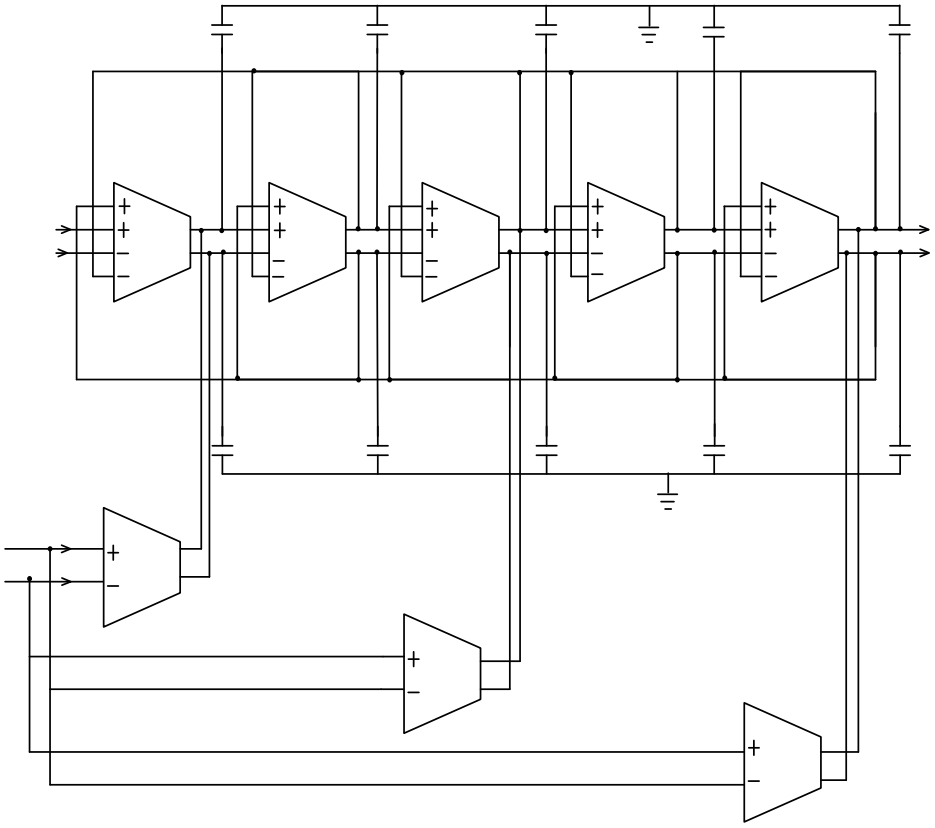


Figure 7.7 Voltage-mode fifth-order IFLF elliptic OTA-C lowpass filter

Writing the circuit voltage transfer function in Figure 7.7 and comparing this function with equation (7.3), the following equations can be established:

$$\tau_1 = B_1, \tau_2 = \frac{B_2}{B_1}, \tau_3 = \frac{B_3}{B_2}, \tau_4 = \frac{B_4}{B_3}, \tau_5 = \frac{B_5}{B_4} \tag{7.8}$$

$$\beta_5 = \frac{A_2}{B_2}, \beta_3 = \frac{A_4}{B_4}, \beta_1 = A_0 \tag{7.9}$$

where $\beta_j = g_{\alpha j}/g_j$, the normalized characteristic of a fifth-order elliptic lowpass filter with 50dB of stopband attenuation and 0.5dB of passband ripple is given in equation (7.6):

Using equations (7.6), (7.8) and (7.9), the time constant τ and zero parameters β can be calculated as [106, 107]:

$$\tau_5 = 0.862\ ,\ \tau_4 = 0.576\ ,\ \tau_3 = 1.431\ ,\ \tau_2 = 1.587\ ,$$
$$\tau_1 = 3.5012\ ,\ \beta_5 = 0.02\ ,\ \beta_3 = 0.11\ ,\ \beta_1 = 1$$

For the identical g_j (j=1 to 5) of 4.5mS, the capacitor values and additional input distribution OTAs can be further calculated as:

$$C_5 = 41.16pF,\ C_4 = 27.5pF,\ C_3 = 68.33pF,$$
$$C_2 = 75.77pF,\ C_1 = 167.17pF, g_{a5} = 90\mu S,$$
$$g_{a3} = 495\mu S,\ g_{a1} = 4.5mS$$

7.3.4 Voltage-mode LF Configuration

The voltage-mode fifth-order MLF IFLF elliptic OTA-C lowpass filter is shown in Figure 7.8. The detailed design formulae for the general voltage-mode LF configuration were proposed in [118, 119, 127]. The transfer function for the voltage-mode fifth-order elliptic lowpass filter in Figure 7.8 is given by:

$$N(s) = \beta_1\tau_2\tau_3\tau_4\tau_5 s^4 + [\beta_1(\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5) + \beta_3\tau_4\tau_5]s^2 + (\beta_1 + \beta_3 + \beta_5)$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1$$

Comparing with equation (7.3), the following values can be obtained:

$$\tau_5 = \frac{B_5}{B_4}, \tau_4 = \frac{B_4}{B_3 - B_2\tau_5}, \tau_3 = \frac{B_3 - B_2\tau_5}{B_2 - (B_1 - \tau_5)\tau_4}, \tau_2 = \frac{B_2 - (B_1 - \tau_5)\tau_4}{B_1 - \tau_5 - \tau_3}, \tau_1 = B_1 - \tau_5 - \tau_3,$$
$$\beta_5 = \frac{A_4}{B_4}, \beta_3 = \frac{A_2 - 2\beta_5 B_2}{\tau_2\tau_1}, \beta_1 = A_0 - (\beta_3 + \beta_5)$$

(7.10)

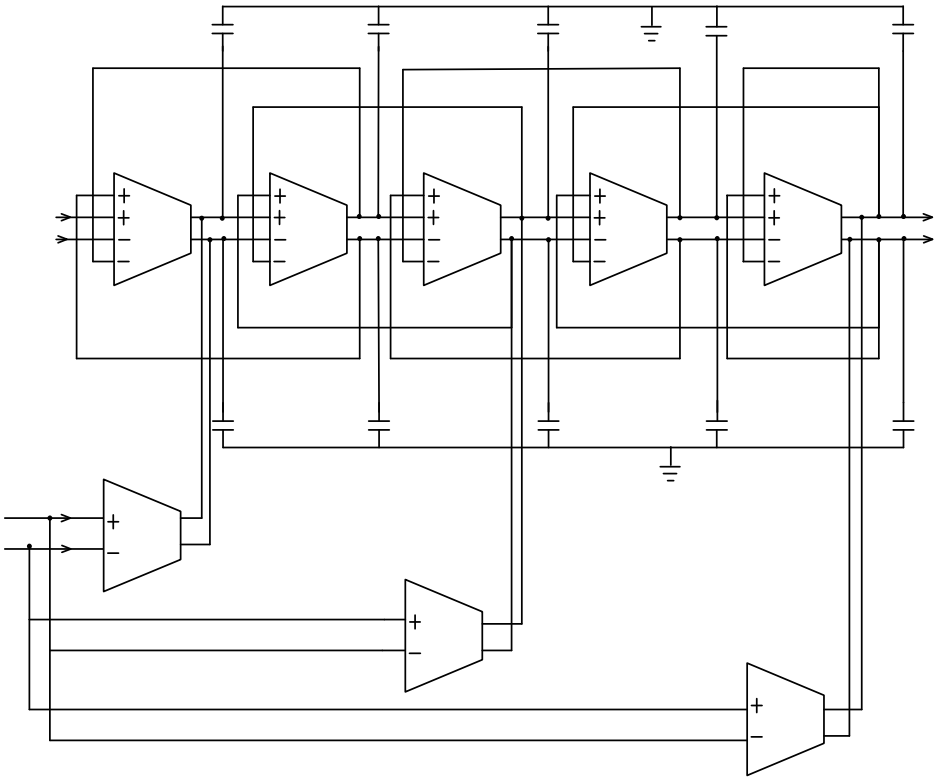


Figure 7.8 Voltage-mode fifth-order LF elliptic OTA-C lowpass filter

The normalized characteristic of a 60dB stopband rejection, 1dB passband ripple fifth-order elliptic lowpass filter is given by equation (7.7):

Using equation (7.7) and (7.10), time constant τ and zero parameters can be calculated as:

$$\tau_5 = 0.858, \tau_4 = 1.44, \tau_3 = 1.829, \tau_2 = 1.802, \tau_1 = 1.152,$$
$$\beta_5 = 0.004, \beta_3 = 0.132, \beta_1 = 0.864$$

For identical g_j (j=1 to 5) of 4.5mS, we can further calculate:

$$C_5 = 41\ pF, C_4 = 68.75\ pF, C_3 = 87.33\ pF,$$
$$C_2 = 86.01\ pF, C_1 = 55\ pF, g_{a5} = 18\ \mu S, g_{a3} = 594\ \mu S,$$
$$g_{a1} = 3.9\,mS$$

a

g_1

b

7.4 Simulation Results

7.4.1 Simulation Results of Current-mode Elliptic OTA-C Lowpass Filters

The circuits were simulated using BSIM 3v3 Spice models for a TSMC 0.18μm CMOS process available from MOSIS [112, 113]. Figure 7.9 shows the open circuit DC gain of presented OTA with and without output resistance compensation. As can be seen, the DC gain of the OTA with negative resistance load is about 72dB, while without negative resistance load, it is only about 22dB.

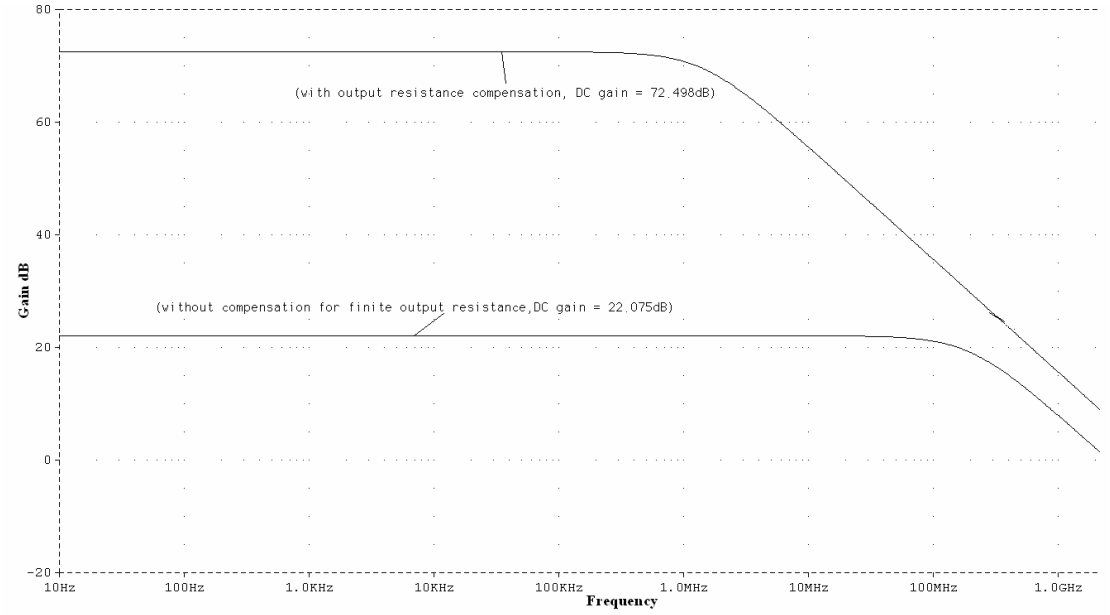


Figure 7.9 Simulated open circuit DC gain of OTA with and without output resistance compensation

Figure 7.10 and 7.11 show the magnitude responses of the FLF and LF filter, respectively. The passband ripple of both filters is in Figures 7.12 (FLF) and 7.13 (LF). The passband ripple of FLF and LF configurations is about 0.5dB and 0.7dB respectively. The stopband attenuation of FLF and LF configurations is about 50dB and 65dB, respectively, matching the expected goals.

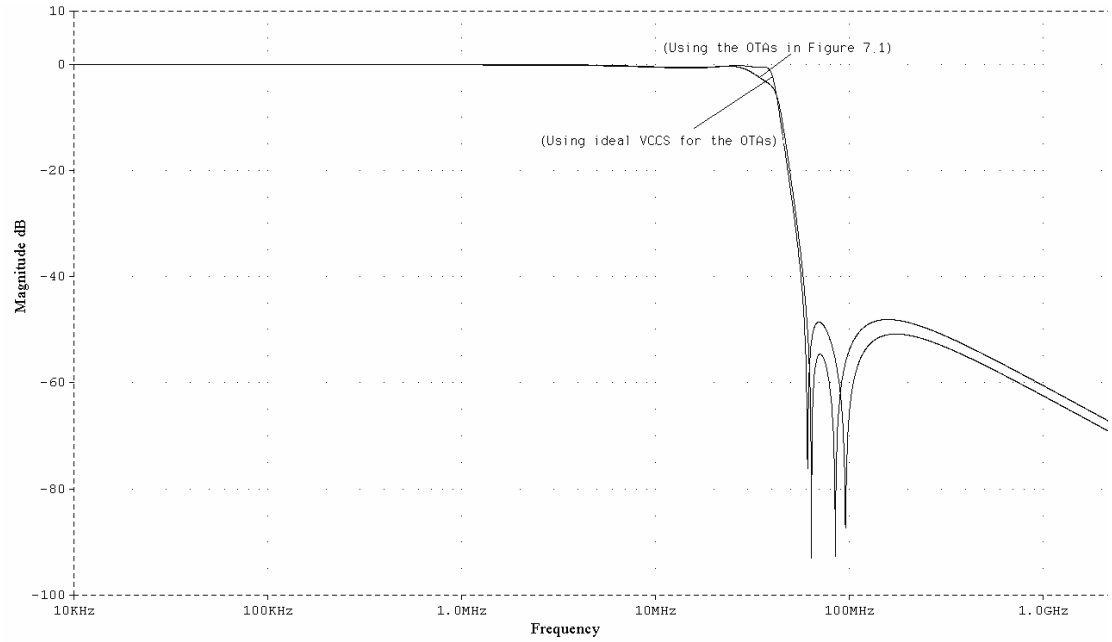


Figure 7.10 Simulated magnitude frequency response of the current-mode fifth-order FLF elliptic lowpass filter

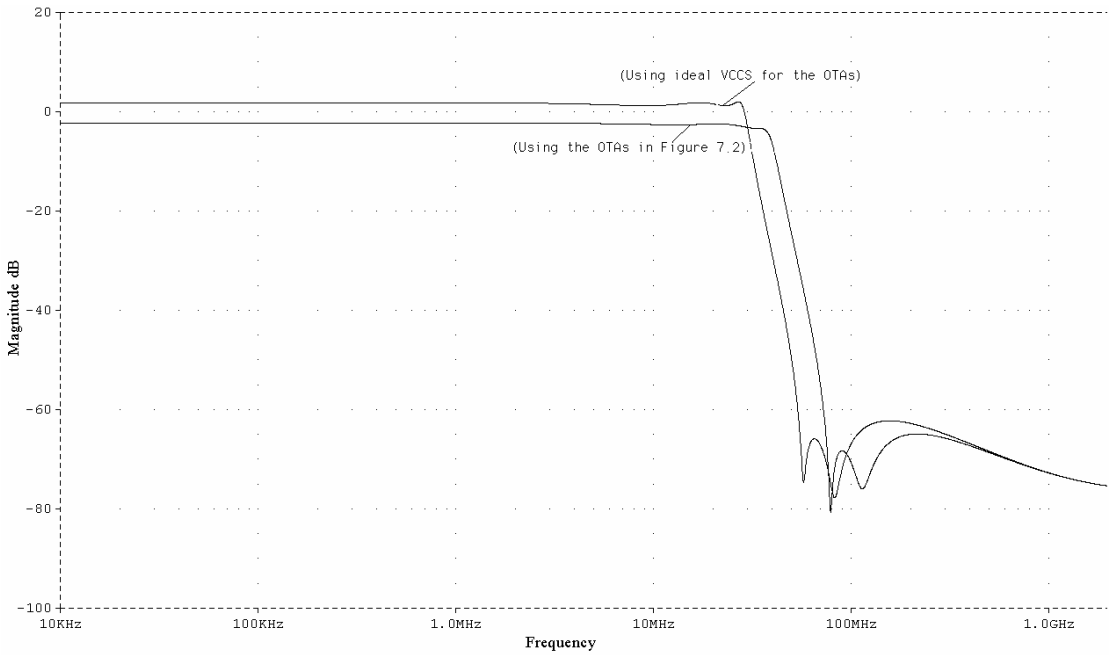


Figure 7.11 Simulated magnitude frequency response of the current-mode fifth-order LF elliptic lowpass filter

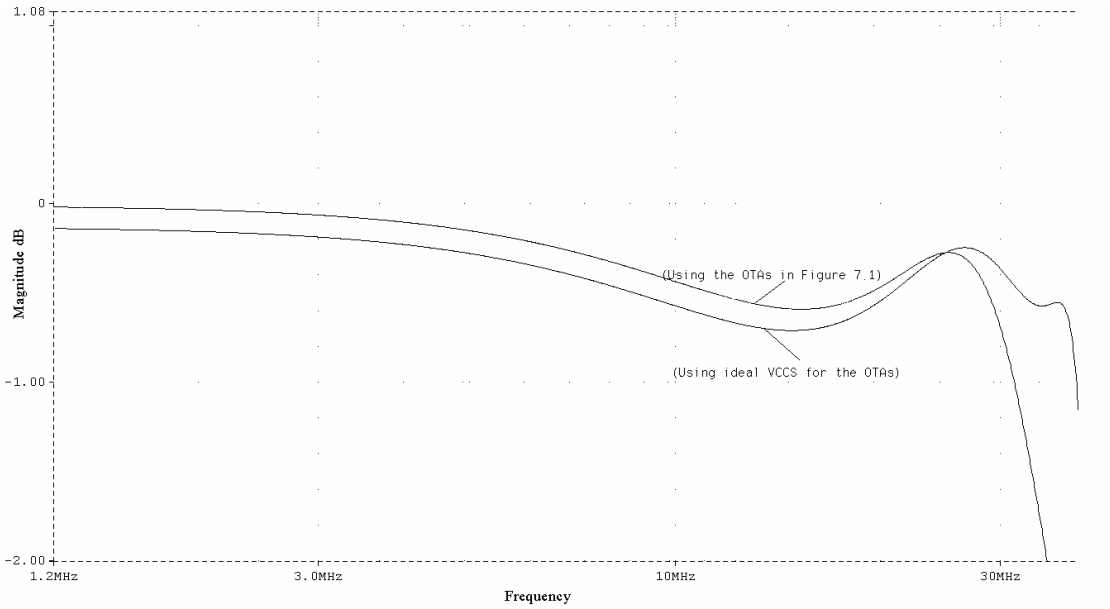


Figure 7.12 Simulated the passband ripples of the current-mode fifth-order FLF elliptic lowpass filter

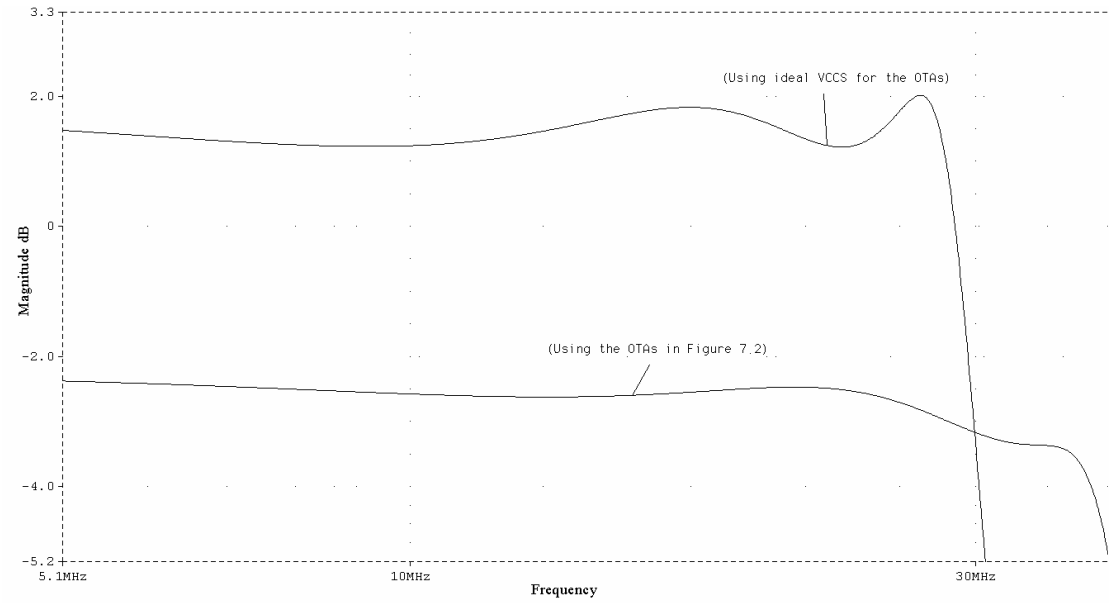


Figure 7.13 Simulated the passband ripples of the current-mode fifth-order LF elliptic lowpass filter

The total RMS output noise current integrated over 30MHz of the LF and FLF filter is about 300nA$_{RMS}$ and 280nA$_{RMS}$, respectively. As also can be seen from Figure 7.14 and 7.15, the THD of both filters can be guaranteed less than 1% at 670uA differential

input current.

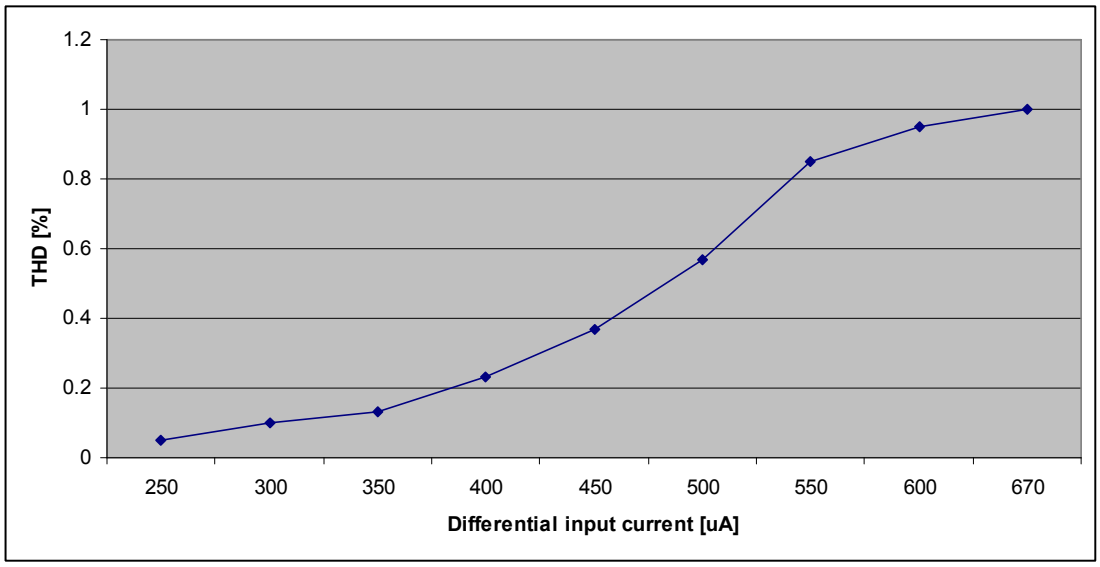


Figure 7.14 Simulated THD versus the differential input current of the current-mode fifth-order LF elliptic lowpass filter

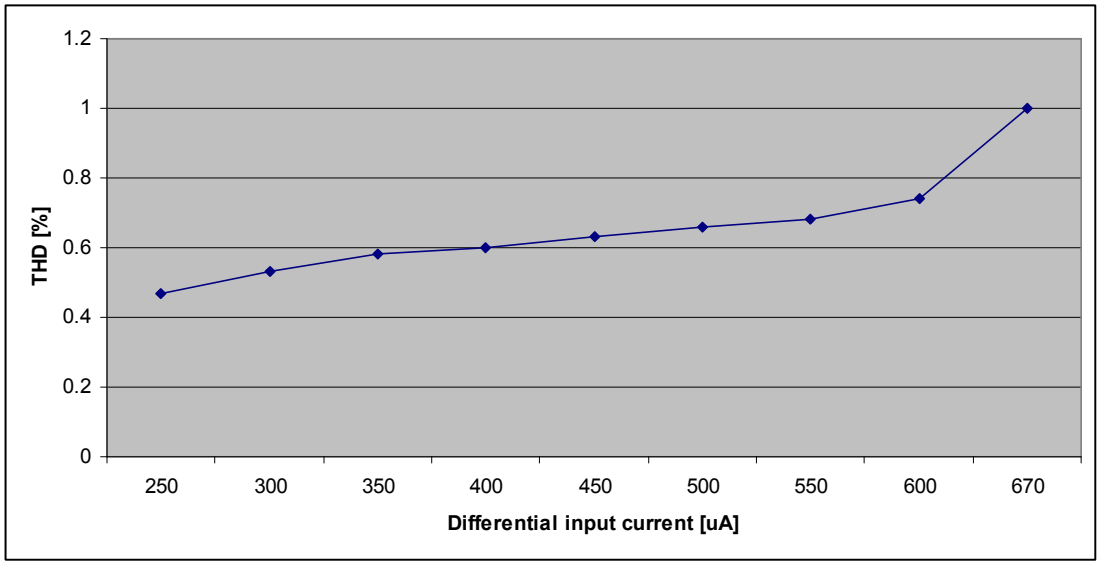


Figure 7.15 Simulated THD versus the differential input current of the current-mode fifth-order FLF elliptic lowpass filter

The dynamic range is about 67dB at f_c=30MHz. The cut-off frequencies of both filter configurations can be tuned from 28MHz to 44MHz. The total power consumption of both filters is about 67mW at 30MHz cut–off frequency for a single 1.8V power supply.

7.4.2 Simulation Results of Voltage-mode Elliptic OTA-C Lowpass Filters

The circuits for the voltage-mode elliptic OTA-C lowpass filter implementations were also simulated using the BSIM 3v3 Spice models for the same TSMC 0.18μm CMOS process. As can be seen from Figures 7.16 and 7.17, the magnitude responses of the voltage-mode fifth-order OTA-C elliptic lowpass filters have similar features to their current-mode counterparts.

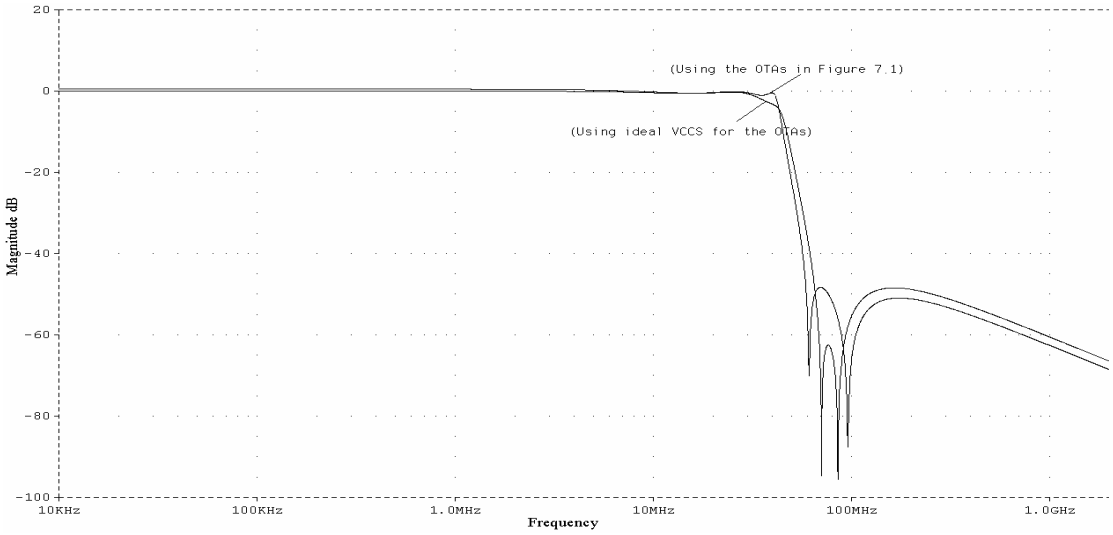


Figure 7.16 Simulated magnitude frequency response of the voltage-mode fifth-order IFLF elliptic lowpass filter

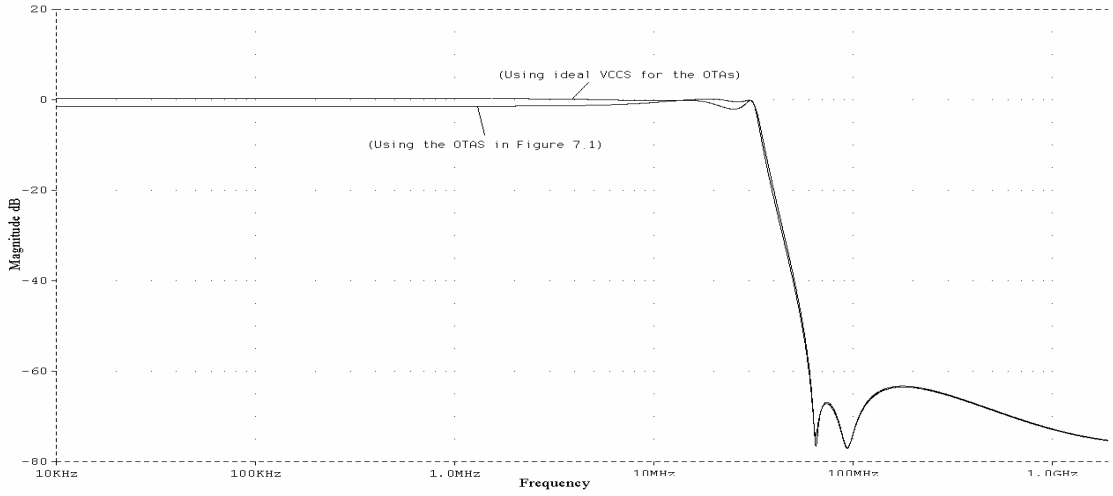


Figure 7.17 Simulated magnitude frequency response of the voltage-mode fifth-order LF elliptic lowpass filter

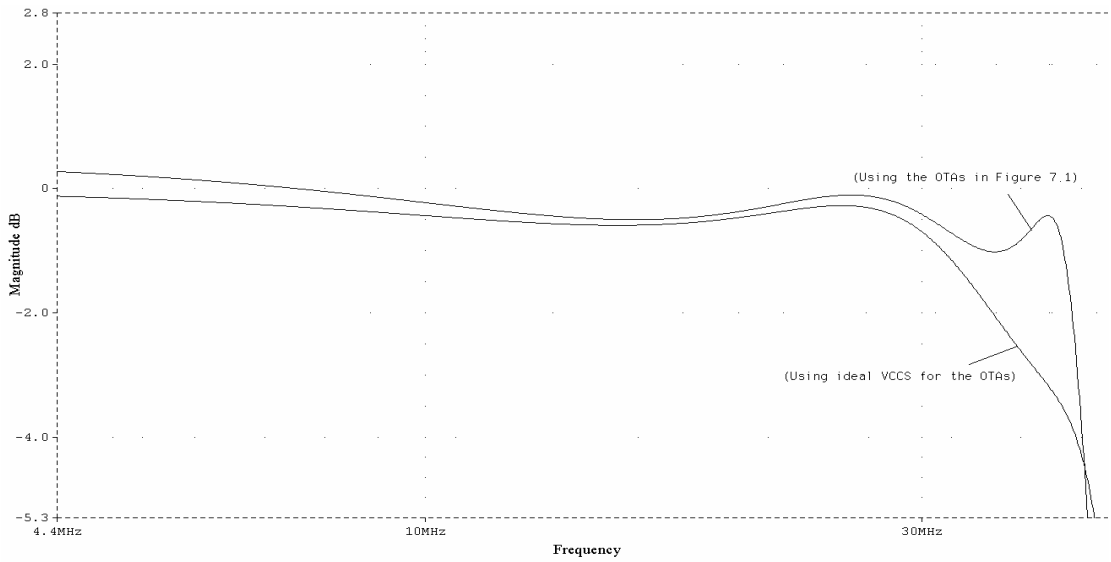


Figure 7.18 Simulated the passband ripples of the voltage-mode fifth-order IFLF elliptic lowpass filter

The passband ripple of the IFLF and LF voltage-mode filters are presented in Figure 7.18 and 7.19, respectively. Figure 7.18 shows the passband ripple of the IFLF filter is about 0.9dB. In Figure 7.19, the passband ripple of the LF filter is about 1.5dB.

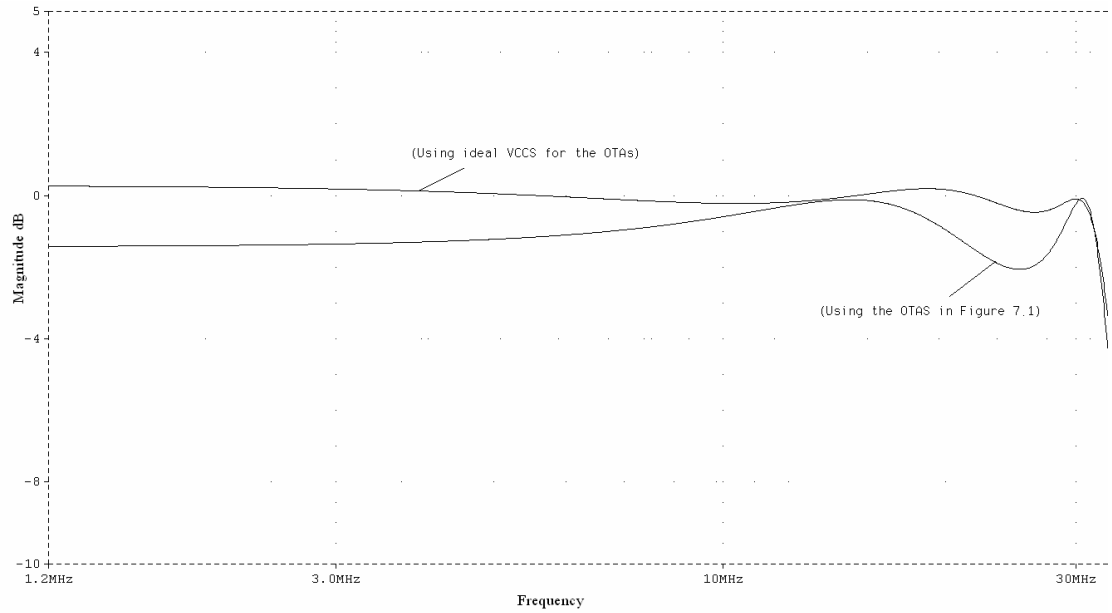


Figure 7.19 Simulated the passband ripples of the voltage-mode fifth-order LF elliptic lowpass filter

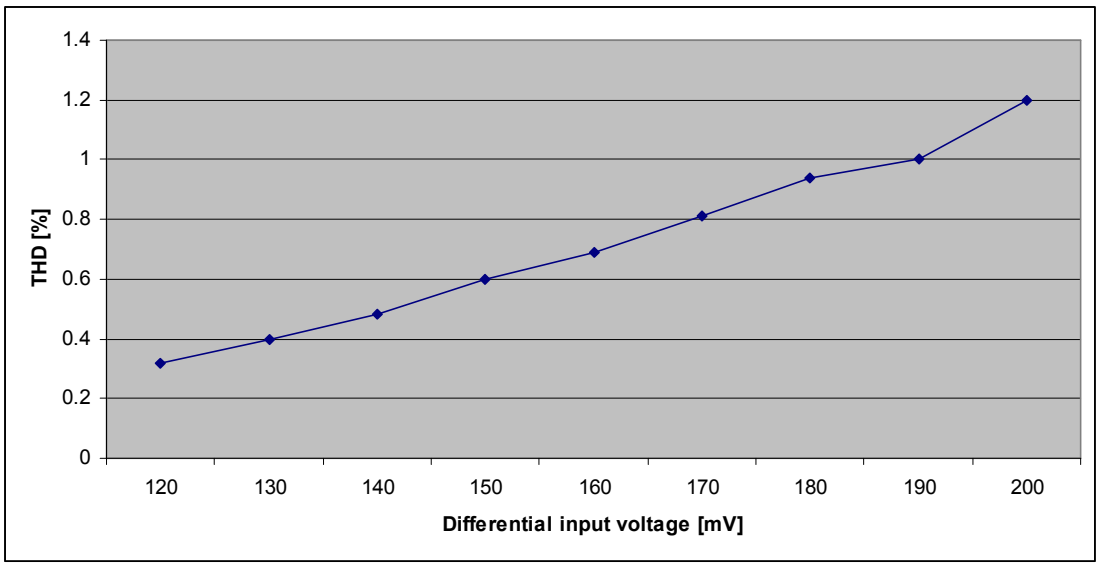


Figure 7.20 Simulated THD versus the differential input voltage of the voltage-mode fifth-order LF elliptic lowpass filter

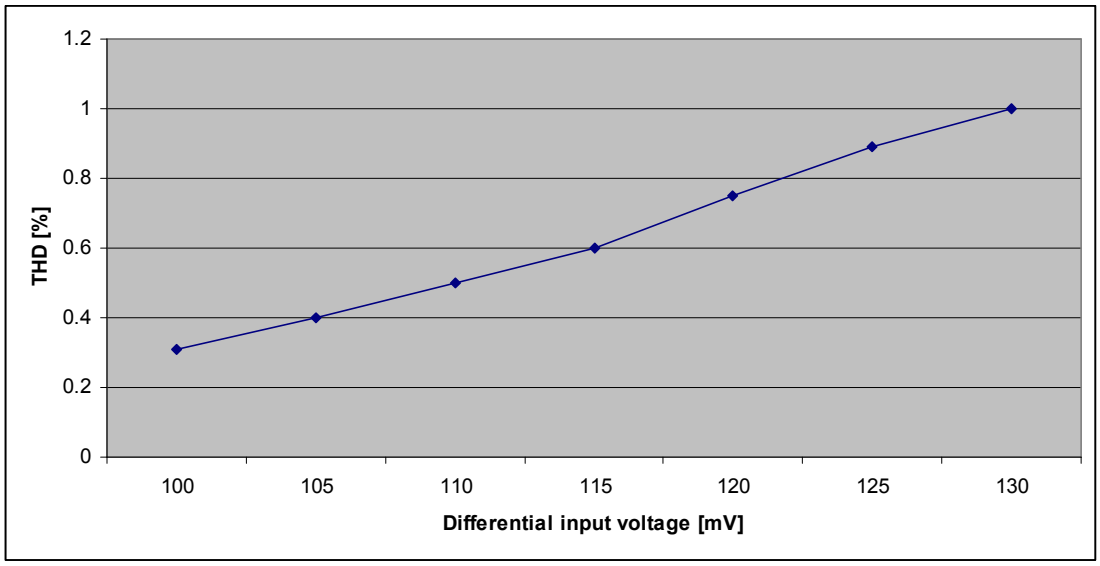


Figure 7.21 Simulated THD versus the differential input voltage of the voltage-mode fifth-order FLF elliptic lowpass filter

The output noise voltage spectrum of the voltage-mode LF and IFLF filters at the cut-off frequency is about $14.5uV_{RMS}/\sqrt{Hz}$ and $18uV_{RMS}/\sqrt{Hz}$, respectively. It yields that the input referred noise is $280uV_{RMS}$ and $350uV_{RMS}$, respectively. The comparison of the simulated current-mode LF and FLF filters with target

specifications are summarized in the Table 7.1 and 7.2, respectively.

Table 7.1 Comparison of the simulated current-mode LF filter with target specifications

Specification for LF	Dynamic range	Power consumption	Cut-off frequency	Passband ripple	Stopband rejection
Target	60dB	80mW	30MHz	1dB	60dB
Simulation	67dB	67mW	28-44MHz	0.7dB	65dB

Table 7.2 Comparison of the simulated current-mode FLF filter with target specifications

Specification for FLF	Dynamic range	Power consumption	Cut-off frequency	Passband ripple	Stopband rejection
Target	60dB	80mW	30MHz	0.5dB	50dB
Simulation	62dB	67mW	28-44MHz	0.5dB	50dB

7.5 Conclusions

The fully-differential fifth-order current- and voltage-mode MLF OTA-C elliptic lowpass filter configurations has been presented. The model presented is also suitable for realization of any arbitrary zeros by adding either voltage, current input distribution or voltage, current output summation OTA networks to it. It is interesting to note that the general current-mode fully-balanced model based on current integrators and current amplifiers have the same form of transfer function as that based on voltage integrators and voltage amplifiers. This can also be explained by noting that voltage-mode OTA-C filters and current-mode OTA-C filters in this chapter are adjoint of each other.

Two CMOS 30MHz current-mode fifth-order elliptic lowpass filter based on MLF FLF LF configurations have been firstly described in this Chapter. A linear OTA with a transconductance of 4.5mS has been used for all the designs. Simulation results in 1.8V 0.18μm CMOS have shown the frequency range of 28-44MHz, dynamic range of 67dB, 62dB and 280nA$_{RMS}$, 300nA$_{RMS}$ total output noise with 67mW of total power consumption at 30MHz of cut-off frequency for current-mode elliptic OTA-C MLF LF FLF lowpass filters, respectively. Simulation results have also shown the voltage-mode elliptic OTA-C MLF LF IFLF lowpass filters have the similar performance as the current-mode ones. Therefore, it has demonstrated that MLF configurations are easy to design elliptic filters and the results also have shown that the proposed filters can be used for advanced wireless receivers.

8. Conclusions

This thesis has investigated design, performance analysis and comparison of CMOS MLF OTA-C filters. Chapter 1 has generally introduced the research background. Chapter 2 has reviewed and summarized the developments in analogue filter design for computer HDD read channels. Chapter 3 has been concerned with design and performance analysis of current-mode FLF and voltage-mode IFLF VHF OTA-C linear phase filters for hard disk read channels, including design of a high performance OTA. The synthesis and design of LF OTA-C filters have been thoroughly investigated in Chapter 4. In Chapter 5, we have designed two UHF fifth-order current- and voltage-mode LF OTA-C hard disk read channel filters; 750MHz cut-off frequency with relatively low power consumption for both filters have been achieved. Chapter 6 overviewed the recent developments of analogue filters design for wireless communication receivers with focus on the multi-standard application. The design details of fifth-order current- and voltage-mode HF elliptic OTA-C filters based on LF, FLF and IFLF structures for wideband wireless baseband applications have been given in Chapter 7. This chapter will summary the work in the thesis (Section 8.1) and propose some further research topics (Section 8.2).

8.1 Summary of the Work

In Chapter 2, the design considerations for high performance analogue filters for HDD systems have been presented. The choices of OTAs, filter orders, filter approximations, and filter architectures by considering their advantages and disadvantages have been addressed. Design trade-offs in relation to power consumption, speed, group delay ripples and large tuning range have also been given. The design considerations presented in this chapter can serve as useful practical guidelines for engineers to design low cost, compact, low power, highly integrated and high performance analogue filters. This Chapter has provided the HDD application background and requirements for the subsequent Chapter 3 to Chapter 5.

In Chapter 3, the synthesis and derived formulae of current-mode OTA-C filters have been presented. The transmission zeros can be implemented using either an input distribution network or output summation network. The input distribution networks have been implemented with voltage-mode IFLF and LF configurations previously. Therefore, the output summation networks have been chosen in this Chapter. We have proposed an OTA based on source degeneration topology, which can balance the trade-offs between power consumption and linearity. The proposed OTA also has typical high frequency and large transconductance features. The design details of the seventh-order current-mode FLF and voltage-mode IFLF 0.05° equiripple linear phase lowpass OTA-C filters and the fifth-order current-mode FLF 0.05° equiripple linear phase lowpass OTA-C filter have been given. The detailed performance analyses of these current- and voltage-mode filters have been included as well. Simulation results in a standard TSMC 0.18μm CMOS process with a 2/2.5V power supply have shown that the proposed fully-differential FLF and IFLF OTA-C lowpass filters have low power consumption, although the group delay ripple is slightly higher than the specification of computer HDD read channels. Therefore the FLF and IFLF configurations can be one of the filtering solutions for next generation computer HDD read systems.

In Chapter 4 we have firstly presented the synthesis and explicit design formulas for current-mode LF OTA-C filters. The synthesis and explicit design formulas of the LF filters are based on an alternative iterative approach. We have formulated the circuit transfer functions and iterative design formulas of all-pole and transmission zero (with both input distribution OTA network and output summation OTA network) LF filters. In this chapter, we have also presented the design of a CMOS 650MHz seventh-order 0.05^{o} equiripple linear phase LF lowpass filter for computer HDD read channel. The simulation results of the CMOS OTA and the LF filter in a standard TSMC 0.18μm CMOS process have also been presented. Simulations results with a single 2.5V supply voltage have shown that the filter has attractive high frequency performance with reasonable group delay ripples, which is the key point for next

generation HDD read channels. However, the power consumption of the proposed filter is relatively high. Therefore, more research has been carried in Chapter 5 to balance the trade-off between power consumption and high frequency performance. .

In Chapter 5, we have presented two high performance LF lowpass OTA-C filters; voltage- and current-mode fifth-order 0.05° equiripple linear phase lowpass filters. The voltage-mode filter has the cut-off frequency of 790MHz and power consumption of 240mW. The group delay ripple is around 4% with and without gain boost. The frequency tuning range is from 455MHz to 790MHz. The programmable gain boost of 6dB has also been achieved. The current-mode filter has also achieved the relatively similar performances. Both theoretical and transistor level (conducted with a standard TSMC 0.18μm CMOS process) results have shown that the LF configuration can also be one of the filtering solutions for next generation HDD read channels. In the chapter, the performance analysis including DC response, frequency performances and second-order effects of a tunable fully-differential CMOS has also been presented in details. Simulation results of the OTA in the same CMOS process with a 1.8V power supply have been given.

In Chapter 6, we have summarized the design considerations of analogue baseband lowpass filters for use in multi-standard receivers based on the direct conversion architecture. Design trade-offs in relation to power consumption, linearity, silicon area, and large tuning range have been discussed. Although active-RC structures have been widely used nowadays, OTA-C filter structures will attract more attention in the near future, especially for wideband wireless applications due to their high frequency capability. The limited linearity can be further improved by integrated resistors or other OTA linearization techniques. Although suitable lowpass filters can be implemented by BiCMOS, SiGe or a combination of these technologies, monolithic implementations using pure CMOS technology remains highly desirable for future communication systems design. A CMOS MLF fourth-order current-mode Butterworth OTA-C lowpass filter was designed as an illustrative example for analogue baseband filtering. The simulation results well match the desired goals for

operation with the Bluetooth, WCDMA and WLAN standards. With the convergence of communications, broadcasting and computing, future mobile terminal or handset must be highly programmable to accommodate any emerging standards. A high performance analogue filter system with a reconfigurable architecture and tunable parameters will thus be needed.

Recent wireless standards require the bandwidth of analogue baseband to be in the range of 30-40MHz. OTA-C filters are more suitable for this HF range than active-RC filters. Therefore, we have designed LF, IFLF and FLF OTA-C lowpass filters of 40 MHz in Chapter 7. These filters have realized the fifth-order elliptic characteristic with the tunable cut-off frequency of 28-42MHz. Simulation results in 1.8V 0.18μm CMOS have shown the dynamic range of 67dB, 62dB and 54pA/√Hz, 47pA/√Hz total output noise with 67mW of total power consumption at 30MHz cut-off frequency for current-mode elliptic OTA-C MLF LF FLF lowpass filters, respectively. Simulation results have also shown the voltage-mode elliptic OTA-C MLF LF IFLF lowpass filters have the similar frequency and dynamic range performance as the current-mode ones. Although the extra OTAs have been connected with the OTA output as negative resistance to enhance the DC gain, the total power consumption is still lower than the most filters proposed in the literature. The LF, IFLF and FLF configurations can also be applied for even higher frequency applications, such as UWB receivers, since all high impedance nodes are connected with grounded capacitors, the parasitic effects can be significantly reduced.

8.2 Topics of Further Research

8.2.1 MLF OTA-C Equalisers with High Gain Boost for Computer HDD Systems

In this thesis we have investigated the design of OTA-C read channel equalizers based on the MLF topology. As mentioned in Chapter 2, these lowpass linear phase filters not only need to achieve UHF/VHF, but also a high gain boost. The maximum

gain boost achieved so far is 24dB. Most OTA-C equalizer can achieve 12dB of gain boost using the cascade method. However, the maximum gain boost of MLF based filters achieved is only 9dB. Therefore, the future research needs to focus on the gain boost enhancement. Although the 24dB of gain boost has been realized in the literature, the group delay ripple is much higher than 5%. It is a great challenge to achieve both linear phase and high gain boost at UHF frequency range with minimum power consumption. Also, note that on-chip automatic tuning is important to overcome filter performance degradation due to parasitics, process variations, tolerances, temperature, and environmental changes. Thus, the design of the equalizers should also incorporate tuning circuitry.

8.2.2 Multi-standard MLF Lowpass OTA-C Filters for Mobile Communication and Television Systems

Other important application areas of OTA-C filters are in telecommunication systems. So far most reported fully-integrated OTA-C filters are based on the LC simulation approach. Motivated by the work in this thesis, the design of OTA-C filters based on the MLF approach for such applications should be further investigated to fully utilize their advantages. Several practical designs for various telecommunication systems and digital TV systems may be investigated. Examples may include design of CMOS poly-phase (complex) MLF OTA-C channel filters (with high image band rejection) for Bluetooth transceivers, CMOS channel-select MLF OTA-C filters for GSM/DECT/UMTS multi-standard receivers, CMOS MLF OTA-C filters for satellite/GPS receivers, and CMOS lowpass video signal smoothing/anti-aliasing filters for digital TV systems. Again, design of on-chip tuning circuitry for the above fully integrated filters is necessary and low voltage and low power operation should be pursued.

8.2.3 Comparison between Voltage- and Current-mode MLF OTA-C Filters

Filter designers and researchers often argue that current-mode circuits offer higher performances than their voltage-mode counterparts. However, it has been reported that there is no clear borderline between the voltage-mode and current-mode circuits and that voltage-mode and current-mode OTA-C filters show the same performance [129]. To verify and justify the argument, we may investigate and compare practically the performances of both voltage- and current-mode OTA-C filters. Comparison of performances between voltage-mode and current-mode OTA-C filters has not been well investigated [130, 131]. The work in [130, 131] was only concerned with second-order voltage-mode and current-mode OTA-C filters, which may not be suitable for high-order filters. Thus, we may compare all performances including sensitivity, distortion, noise, dynamic range, and OTA non-ideality effects of typical high-order voltage-mode and current-mode MLF OTA-C filters. As an example, we may compare the voltage-mode IFLF filter with the equivalent current-mode FLF filter, and the voltage-mode LF filter with the current-mode LF filter.

8.2.4 Design of MLF OTA-C Bandpass Filters for Wireless Communications

In wireless communications transceivers, the bottleneck for a single chip implementation is to bring the RF/IF bandpass channel filters onto the silicon. However, designing very high frequency high Q bandpass filters is extremely challenging [2-4, 67, 68]. No solutions have been found so far. The research will look at the alternatives to the methods already tried in the literature. We propose to use multiple loop feedback biquad-based OTA-C filters in this demanding application. In high frequency and high Q bandpass filters, both frequency and Q tuning are required. The frequency tuning method for LF and IFLF configurations can be found in [2, 3, 9, and 68]. Although some Q tuning methods for cascade and LC ladder simulation

OTA-C filters have been proposed in the literature [2, 3, 9, 65, 67], the Q tuning method for MLF OTA-C filters has not been found so far. Thus, the future work on high Q bandpass filter design using MLF OTA-C filter will also investigate the Q tuning issues.

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Appendix

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.MODEL CMOSN2 NMOS (
LEVEL     = 7
TNOM      = 27
TOX       = 4E-9
XJ        = 1E-7
NCH       = 2.3549E17
VTH0      = 0.3469417
K1        = 0.5824648
K2        = 2.675158E-3
K3        = 0.0152228
K3B       = -10
W0        = 7.540113E-6
NLX       = 1.661475E-7
DVT0W     = 0
DVT1W     = 0
DVT2W     = 0
DVT0      = 1.6323269
DVT1      = 0.4647698
DVT2      = -0.0450965
U0        = 260.3005546
UA        = -1.314002E-9
UB        = 2.099332E-18
UC        = 3.819093E-11
VSAT      = 1.052288E5
A0        = 2
AGS       = 0.3695786
B0        = -1.798439E-8
B1        = -1E-7
KETA      = -0.0162254
A1        = 9.488078E-4
A2        = 1
RDSW      = 150
PRWG      = 0.5
PRWB      = -0.2
WR        = 1
WINT      = 8.920936E-9
LINT      = 2.370607E-9
DWG       = 2.221299E-9
DWB       = -6.313837E-9
VOFF      = -0.0759061
NFACTOR = 2.3433592
CIT       = 0
CDSC      = 2.4E-4
CDSCD     = 0
CDSCB     = 0
ETA0      = 4.938514E-5
ETAB      = -1.936318E-3
DSUB      = 0.0952747
PCLM      = 3.0632837
PDIBLC1 = 0.9823911
PDIBLC2 = 1.275381E-3
PDIBLCB = 0.1
DROUT     = 0.9393639
PSCBE1    = 1E8
PSCBE2    = 7.673156E-10
PVAG      = 2.3385508
DELTA     = 0.01
RSH       = 6.7
MOBMOD    = 1
PRT       = 0
UTE       = -1.5
KT1       = -0.11
KT1L      = 0
KT2       = 0.022
UA1       = 4.31E-9
UB1       = -7.61E-18
UC1       = -5.6E-11
AT        = 3.3E4
WL        = 0
WLN       = 1
WW        = 0
WWN       = 1
WWL       = 0
LL        = 0
LLN       = 1
LW        = 0
LWN       = 1
LWL       = 0
```

```
CAPMOD    = 2
XPART     = 0.5
CGDO      = 7.2E-10
CGSO      = 7.2E-10
CGBO      = 1E-12
CJ        = 9.908001E-4
PB        = 0.7382604
MJ        = 0.3578423
CJSW      = 2.417604E-10
PBSW      = 0.5261825
MJSW      = 0.1199858
CF        = 0
PVTH0     = 1.232879E-3
PRDSW     = -5
PK2       = -1.180394E-3
WKETA     = -3.479546E-3
LKETA     = 7.451244E-4
PVSAT     = 2E3
PETA0     = 1E-4
PKETA     = 1.888841E-4        )
*$


.model MbreakP-X10 PMOS
LEVEL     = 7
TNOM      = 27
TOX       = 4E-9
XJ        = 1E-7
NCH       = 4.1589E17
VTH0      = -0.4018217
K1        = 0.5542041
K2        = 0.0344339
K3        = 0
K3B       = 10.2986
Dwg= -2.6442e-8
Dwb= -5.4435e-8
rsh= 7.5
Dvt0= 0.5159
Dvt1= 0.2828
Dvt2= 0.1
Dvt0w= 0.00
Dvt1w= 0.00
Dvt2w= 0.00
Nlx= 9.5035e-8
W0= 1e-6
Vsat= 1.496e5
Ua= 1.594e-9
Ub= 1.125e-21
Uc= -1e-10
Prwb= -0.1249
Prwg= 0.5
Wr= 1.0000000
U0=116.67
A0= 1.6385
Keta= 0.02125
A1= 0.4245
A2= 0.4836
Ags= 0.3897
B0= 1.536e-6
B1= 4.912e-6
Voff=-0.09768
NFactor= 1.997
Cit= 0.00
Cdsc= 2.4e-4
Cdscb= 0.00
Cdscd= 0.00
Eta0= 0.1387
Etab= -0.2049
Dsub= 1.245
Pclm=2.297
Pdiblc1= 8.033e-4
Pdiblc2= 0.01373
Pdiblcb= -1e-3
Drout= 0
Pscbe1= 2.444e9
Pscbe2= 7.06e-10
Pvag= 12.65
Delta= 1.0000000E-02
kt1= -0.11
kt2= 0.022
At= 3.3E+04
Ute= -1.5
Ua1= 4.31e-9
Ub1= -7.61e-18
Uc1= -5.6e-11
Kt1l= 0
```

Prt= 0.00
Cj= 1.182e-3
Mj= 0.4163
Pb= 0.8684
Cjsw= 1.922e-10
Mjsw= 0.3
Cgdo=6.73e-10
Cgso=6.73e-10
Cgbo=1e-12
Capmod= 2
Xpart= 0.5
Cf= 0.00
mobmod=1
pbsw=0.6322
rdsw = 354.7
wint = 1.17e-8
lint = 2.17e-8
pbsw = 0.6322
pvth0 = 2.703e-3
PRDSW = 0.6067904
PK2 = 3.126202E-3
WKETA = 0.0406736
LKETA = -2.070108E-3
*$