Switched-current filter structure for synthesizing arbitrary characteristics based on follow-the-leader feedback configuration

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Abstract A switched-current (SI) filter structure with follow-the-leader feedback configuration has been proposed for synthesizing arbitrary transfer functions. The double-sampling fully-balanced SI bilinear integrator and current mirror are employed as the building cells in order to enhance overall performance and make circuit design more flexible. Also, explicit design formulas are derived by using coefficient matching. The third-order low-pass and band-pass filter are designed as the examples. Simulation results confirm that the presented filter structure is very suitable for the operation with high sampling-to-cutoff frequency ratio, and can synthesize arbitrary filter characteristics precisely and easily while keeping low sensitivity.

Keywords Switched-current filter • Multiple-loop feedback • Bilinear transform • Double-sampling fully-balanced • Follow-the-leader feedback configuration

1 Introduction

Switched-current (SI) filter has attracted much attention over the past few decades [1]. Compared with continuous-time filter [2-9], the time constant of SI filter can be fabricated accurately in the IC process, since the time constant depends on the well-matched values of the same kind of components, i.e. MOSFET aspect ratio. Also, SI filter has been considered as an alternative to switched-capacitor (SC) filter in mixed signal systems, owing to the characteristic of compatibility with digital VLSI technology. To date, several competitive SI basic cells have been presented [10-16]. However, the generation of SI filter structure has not been investigated well so far, which has greatly impeded the widespread application of SI technique. Till now, only a few SI filter structures have been proposed, among which the LC ladder simulation structure [17,18] is considered as the optimum choice due to the lower magnitude sensitivity compared with cascade [19] and parallel [20] structures. Albeit successful in many aspects, the ladder simulation methods are normally based on a particular passive RLC prototype and can only realize limited transmission zeros [21], thus being not general enough for synthesizing the transfer function with non-conventional zeroes. In addition, the ladder simulation methods need knowledge of passive RLC filters, and do not have explicit design formulas, which have become an obstacle for nonspecialist SI designers to conduct rapid and accurate filter realization.

Under this background, this Letter aims to propose an SI filter structure with general applicability, simple synthesis procedure and explicit design formulas. To achieve this goal, the SI filter structure with follow-the-leader feedback (FLF) configuration is presented, and bilinear SI integrator is employed as the building cell. It should be noted that unlike in the continuous-time filter design, discrete-time multiple loop feedback SI filters have not been investigated as a general methodology. Although a FLF SI structure was first used in wavelet filter design [22], it has several shortcomings for practical implementation as will be commented later. This Letter proposes a novel realization structure by using several enhancement techniques, e.g. employing double-sampling fully-balanced configuration and introducing more design variables to obtain realizable circuit parameters.

2 Proposed SI filter structure

2.1 Building cells

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As the sampled-data technique, SI filters need to be synthesized through performing z-transform on the transfer function given in s-plane, i.e.

$$H(s)=\frac{A_{n-1}s^{n-1}+A_{n-2}s^{n-2}+\cdots+A_1s+A_0}{s^n+B_{n-1}s^{n-1}+B_{n-2}s^{n-2}+\cdots+B_1s+B_0} \quad (1)$$

Bilinear z-transform can guarantee stability and avoid amplitude distortion, thus SI bilinear integrator (BI) is selected as the building block. Fig.1(*a*) gives the universal structure for employed double-sampling fully-balanced SI BI operated with two non-overlapping phase ϕ_1 and ϕ_2, in which M_i and its associated bias current source J constitute the integrator core. Herein, M_i is symbolized by black box for generality, and represents the elementary current memory, which samples input current on phase ϕ_i and sustains on the next phase. Simply, M_i can be realized by an NMOS transistor with associated switch closed on phase ϕ_i [10], the so-called second generation SI memory cell. But, for cancelling non-ideal behaviour, several enhancement techniques such as cascode and S^2I can be used [10-16]. Particularly, when S^2I technique is selected to realize M_i and J, Fig.1(*a*) can be specialized to the structure used in [17,18].

On phase ϕ_1 of clock period (n-1), balanced input currents i^+ and i^- flow into the left and right single-ended integrator cell, respectively. M_1 samples current and M_2 sustains the current stored on phase ϕ_2 of clock period (n-2). Thus, the currents flowing in M_1 and M_2 have the relationship as below:

$$i_{1L}(n-1)=2J+i^+(n-1)-i_{2L}(n-1) \quad (2)$$

$$i_{1R}(n-1)=2J+i^-(n-1)-i_{2R}(n-1) \quad (3)$$

On phase ϕ_2 of clock period n, balanced input currents i^+ and i^- flow into the right and left single-ended integrator cell, respectively. M_1 sustains the current stored on phase ϕ_1 of clock period (n-1), i.e.

$$i_{1L}(n)=i_{1L}(n-1) \quad (4)$$

$$i_{1R}(n)=i_{1R}(n-1) \quad (5)$$

M_2 samples current, which can be expressed as

$$i_{2L}(n)=2J+i^-(n)-i_{1L}(n) \quad (6)$$

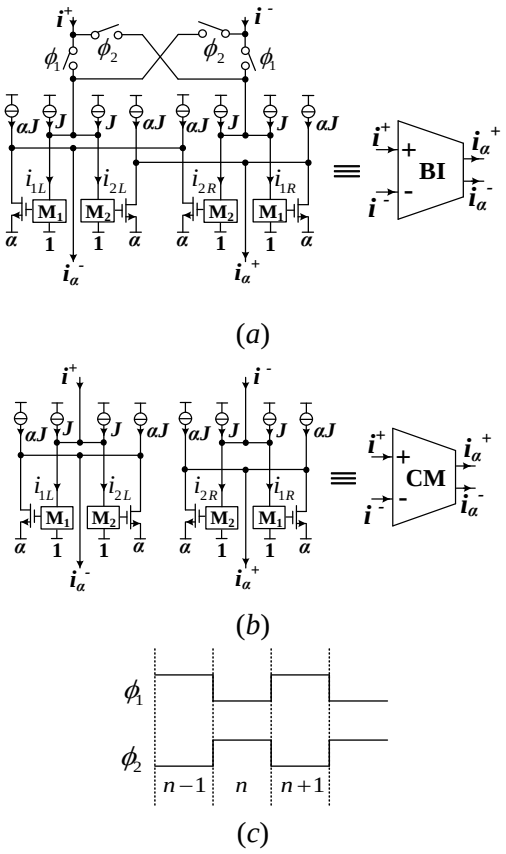
$$i_{2R}(n)=2J+i^+(n)-i_{1R}(n) \quad (7)$$

Then, the balanced output currents i_α^+ and i_α^- can be given as

$$i_\alpha^+(n)=2\alpha J-\alpha i_{2L}(n)-\alpha i_{1R}(n) \quad (8)$$

$$i_\alpha^-(n)=2\alpha J-\alpha i_{1L}(n)-\alpha i_{2R}(n) \quad (9)$$

where integrator coefficient α is defined by the current mirror ratio between the transistor in the integrator core and that at the output.



(*a*)

(*b*)

(*c*)

Fig.1 Building cells of SI filter (*a*) bilinear integrator, (*b*) current mirror, (*c*) phase sequence

Substituting (2)-(7) into (8) and (9), one can deduce that

$$i_\alpha^+(n)=i_\alpha^+(n-1)-\alpha[i^-(n)-i^+(n-1)] \quad (10)$$

$$i_\alpha^-(n)=i_\alpha^-(n-1)-\alpha[i^+(n)-i^-(n-1)] \quad (11)$$

Denoting $i_\alpha^+=-i_\alpha^-=i_\alpha$ and $i^+=-i^-=i$, one can have that

$$H_{BI}(z)=\frac{i_\alpha(z)}{i(z)}=\alpha\frac{1+z^{-1}}{1-z^{-1}} \quad (12)$$

Observed from (10) and (11), when input signal is common-mode (i.e. $i^+=i^-$), the transfer function of BI cell can be given as

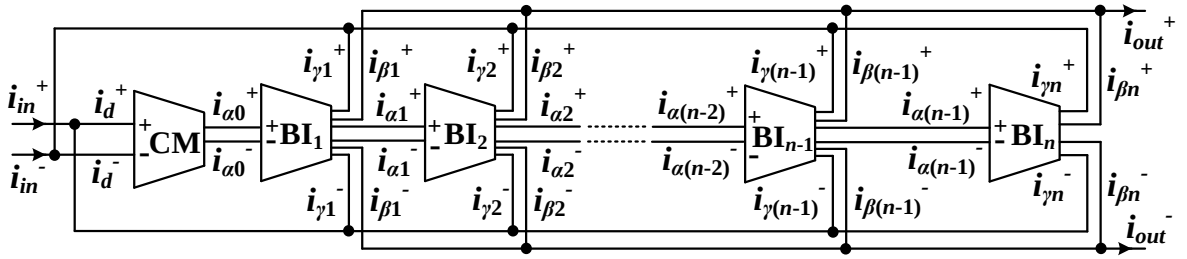


Fig.2 Double-sampling fully-balanced SI filter structure based on FLF configuration

$$H_{BI}(z) = -\alpha \tag{13}$$

which means common-mode signal is not integrated but mirrored to the output with coefficient α.

Another building cell used in this Letter is the double-sampling fully-balanced current mirror (CM). Fig.1(*b*) shows the universal structure of CM, which is constructed from Fig.1(*a*) by eliminating the input switches and changing the output connection. Conducting similar deduction as (2)-(9), the balanced output currents i_α^+ and i_α^- on phase ϕ_2 of clock period n can be calculated as

$$i_\alpha^+(n) = -\alpha i^-(n) \tag{14}$$

$$i_\alpha^-(n) = -\alpha i^+(n) \tag{15}$$

Thus, the transfer function of Fig.1(*b*) can be written as

$$H_{CM}(z) = \frac{i_\alpha(z)}{i(z)} = \alpha \tag{16}$$

2.2 Filter structure and synthesis

Fig.2 shows the proposed double-sampling fully-balanced SI filter structure with FLF and output summation configuration, in which the BI cell has up to three pairs of balanced outputs, i.e. $i_\alpha^\pm$, $i_\beta^\pm$ and $i_r^\pm$. Fig.3 gives the universal structure of employed triple-output BI cell, realized by adding more output transistors with integrator coefficients β and γ in Fig.1(*a*).

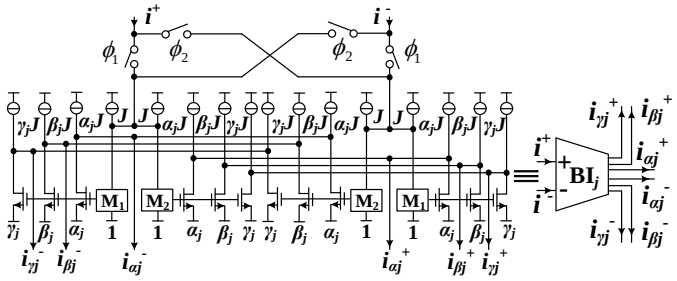


Fig.3 Triple-output bilinear integrator cell

Denoting the normalized output currents of BI$_j$ in Fig.2 as $i_{oj}^\pm$ and assuming $D(z)=(1+z^{-1})/(1-z^{-1})$, then one can have

$$i_{o1} = \alpha_0 i_d D(z),\ i_{oj} = \alpha_{j-1} i_{o(j-1)} D(z)\ \ (j = 2,3,\cdots n) \tag{17}$$

Thus,

$$i_{in} = i_d + \sum_{j=1}^{n} \gamma_j i_{oj} \tag{18}$$

$$i_{out} = \sum_{j=1}^{n} \beta_j i_{oj} \tag{19}$$

Based on (17)-(19), the transfer function of Fig.2 can be obtained as

$$H(z) = \frac{i_{out}(z)}{i_{in}(z)} = \frac{\beta_1\alpha_0 D(z) + \beta_2\alpha_0\alpha_1 D^2(z) + \cdots + \beta_n(\prod_{j=0}^{n-1}\alpha_j)D^n(z)}{1 + \gamma_1\alpha_0 D(z) + \gamma_2\alpha_0\alpha_1 D^2(z) + \cdots + \gamma_n(\prod_{j=0}^{n-1}\alpha_j)D^n(z)} \tag{20}$$

Meanwhile, applying bilinear transform $s = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$ to (1), one can have

$$H_d(z) = \frac{A_{n-1}\frac{T_s}{2}D(z) + A_{n-2}(\frac{T_s}{2})^2 D^2(z) + \cdots + A_0(\frac{T_s}{2})^n D^n(z)}{1 + B_{n-1}\frac{T_s}{2}D(z) + B_{n-2}(\frac{T_s}{2})^2 D^2(z) + \cdots + B_0(\frac{T_s}{2})^n D^n(z)} \tag{21}$$

Using coefficient matching between (20) and (21), the design formulas for the parameters in Fig.2 can be obtained as

$$\begin{aligned} \beta_j &= \frac{A_{n-j}}{\prod_{x=0}^{j-1}\alpha_x}(\frac{T_s}{2})^j \quad (j = 1,2,\cdots,n) \\ \gamma_j &= \frac{B_{n-j}}{\prod_{x=0}^{j-1}\alpha_x}(\frac{T_s}{2})^j \quad (j = 1,2,\cdots,n) \end{aligned} \tag{22}$$

Compared with existing structures, the proposed structure has many advantages as below:

First, the design method and formulas are straightforward and simple to use. Observed from (22), parameters α_j, β_j and γ_j are inter-related. By presetting α_j to be a reasonable value, β_j and γ_j can be easily determined. Herein, the 'reasonable' value for α_j normally means decimal fraction, since common-mode input signal is mirrored to the outputs, and attenuation coefficient α_j gives inherent common-mode rejection. In this way, the

common-mode feedback circuits will not be needed.

Second, the proposed structure can realize arbitrary transfer function. For certain α_j, any coefficients A_j (or zeros) and B_j (or poles) can be realized by selecting proper values of β_j and γ_j based on (22), respectively. It is worth noting that negative β_j can be simply realized by interchanging the related two output terminals with coefficient β_j of BI_j. Specially, if β_j is zero, the related two output terminals of BI_j should be removed. Furthermore, different from the FLF SI structure used in [22], a CM with coefficient α_0 is introduced to make circuit design more flexible. Observed from (22), β_1 and γ_1 are not only determined by fixed values A_{n-1} and B_{n-1}, but also by a design variable α_0. Thus, choosing α_0 properly can guarantee that the calculated β_1 and γ_1 are realizable. Moreover, due to the introduction of α_0, the power of $(T_s/2)^j$ is just equal to the number of design variables, viz. α_x (x=0,1,…, j-1), which means proper choice of α_j can ensure that the calculated β_j and γ_j are not too small to realize as j increases, especially when high sampling-to-cutoff frequency ratio is selected to obtain high-accuracy realization.

Third, double-sampling fully-balanced configuration has superior performance over single-sampling single-ended configuration used in [22]. Unlike single sampling, double sampling processes two samples per clock period, thus can halve the clock frequency, lower memory cell's bandwidth, and enhance signal-to-noise ratio [18]. In addition, single-ended SI filter proposed in [22] employs current mirrors to realize signal inversion, which would introduce excess phase errors and greatly compromise the advantages of bilinear z-transform [18]. Fully-balanced structure does not have this problem, since the signal inversion can be realized simply by interchanging the two input or output terminals of the SI integrator.

3 Design examples

3.1 Low-pass filter

The third-order elliptic low-pass filter with normalized transfer function

$$H(s)=\frac{0.0907s^2+0.2925}{s^3+0.5775s^2+0.9568s+0.2925} \tag{23}$$

is selected as the example. The cutoff frequency of 10kHz and sampling frequency of 100kHz are chosen. To compensate for the distortion brought by bilinear transform, the specified cutoff frequency f_o should be pre-warped by $f_p=(f_s/\pi)\tan(\pi f_o/f_s)$, where f_p and f_s are the pre-warped cutoff and sampling frequency, respectively [1]. For this example, f_p=10.343kHz. Then, the denormalized transfer function has $A_2=5.9100\times10^3$, $A_1=0$, $A_0=8.0813\times10^{13}$, $B_2=3.7613\times10^4$, $B_1=4.0585\times10^9$, $B_0=8.0814\times10^{13}$.

Fig.4 shows the realization circuits using the proposed SI filter structure, in which the coefficients α_j are preset to be α_0=0.2, α_1=0.6, α_2=0.6. Thus, the circuit parameters in Fig.4 can be determined by (22): β_1=0.1478, β_2=0, β_3=0.1403, γ_1=0.9403, γ_2=0.8455, γ_3=0.1403. To testify the feasibility of proposed structure, the second generation SI memory cell is employed in Fig.4. Herein, the ASIZ program [23] is used, which can analyze the frequency response of SI, SC and any periodically switched network easily and conveniently.

Setting the clock frequency 50kHz due to double-sampling operation, Fig.5 plots the magnitude frequency response simulated by ASIZ, along with the ideal response defined by (23). Apparently, the designed filter achieves the desired cutoff frequency, pass-band equiripple and stop-band attenuation. The deviation in high frequency is due to the aliasing effects, which can be reduced by an anti-aliasing filter or higher sampling-to-cutoff frequency ratio. As claimed in section 2.2, the proposed filter structure is well suited for high-accuracy design with high sampling frequency. Selecting f_s=200kHz, for example, the realizable circuit parameters can be obtained by setting α_0=0.1, α_1=0.3, α_2=0.3, whose frequency response is shown in Fig.6. Obviously, the simulated magnitude response is almost the same as ideal response up to 30kHz.

Since the time constant of SI bilinear integrator is in proportion to sampling frequency, the characteristic frequency of SI filter can be tuned precisely and easily by the sampling frequency. As shown in Fig.7, changing the sampling frequency from 200kHz to 100kHz and 400kHz for example, we can realize the SI filter at cutoff frequency of 5kHz and 20kHz, respectively.

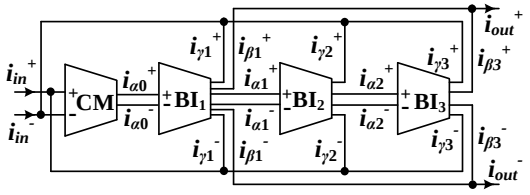


Fig.4 SI structure for third-order low-pass filter

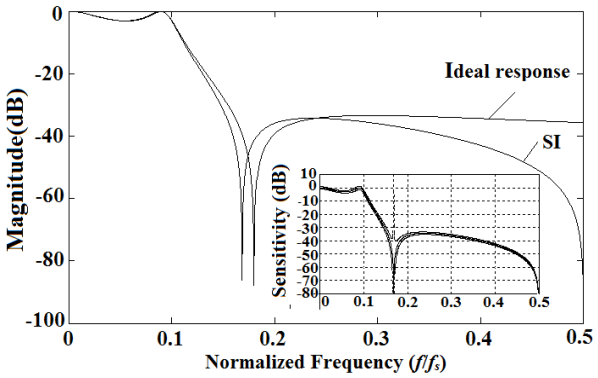


Fig. 5 Magnitude frequency response of low-pass SI filter (f_s=100kHz)

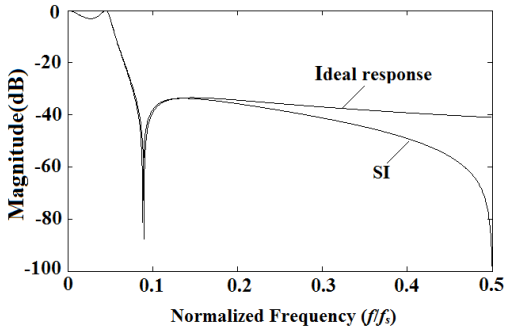


Fig. 6 Magnitude frequency response of low-pass SI filter (f_s=200kHz)

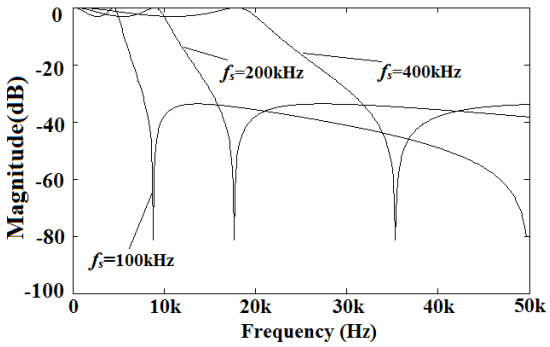


Fig. 7 Low-pass SI filter tuned by sampling frequency

Also, the sensitivity analysis is simulated using ASIZ, computed by assuming 5% random errors in all the transistor transconductances, which is shown as the error margin above and below the nominal gain curve in the small window in Fig.5. Obviously, the proposed structure has low sensitivity in both pass-band and stop-band. The error peak at transmission zero is due to the artifact of computation errors created during sensitivity analysis [23].

3.2 Band-pass filter

The third-order band-pass filter with normalized transfer function

$$H(s)=\frac{0.2403s}{s^3+0.5775s^2+0.9568s+0.2925} \quad (24)$$

is employed as the example. The center frequency of 10kHz and sampling frequency of 100kHz are chosen. Then, the denormalized transfer function has A_2=0, A_1=1.1944×10^9, A_0=0, B_2=4.0714×10^4, B_1=4.7557×10^9, B_0=1.0250×10^{14}.

Fig.8 gives the SI band-pass filter based on the proposed structure. Presetting the coefficients α_j to be identical values 0.4, one can determine the parameters in Fig.8 by (22): β_2=0.1866, γ_1=0.5089, γ_2=0.7431, γ_3=0.2002. Setting the clock frequency 50kHz, Fig.9 shows the magnitude frequency response along with the ideal response defined by (24). The simulated center frequency is almost the same as ideal value 10kHz. The simulated –3dB frequencies of this filter are 8.708kHz and 11.125kHz respectively, which are close to the ideal values (i.e. 8.583kHz and 11.250kHz). As claimed in section 3.1, the deviation in high frequency can be reduced by employing anti-aliasing filter or enhancing the sampling-to-center frequency ratio. The sensitivity analysis is depicted in the small window in Fig.9, which confirms that the proposed SI filter structure has relatively low sensitivity.

By tuning the sampling frequency, one can adjust the center frequency of Fig.8 precisely and easily. Fig.10 shows the magnitude frequency response simulated at sampling frequency of 50kHz, 100kHz and 200kHz, respectively.

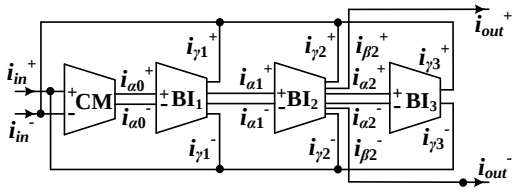


Fig.8 SI structure for third-order band-pass filter

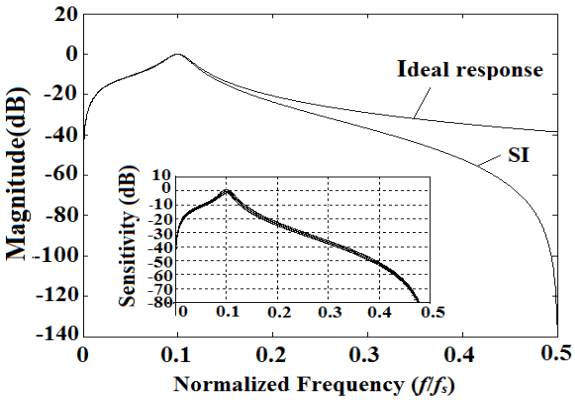


Fig. 9 Magnitude frequency response of band-pass SI filter (f_s=100kHz)

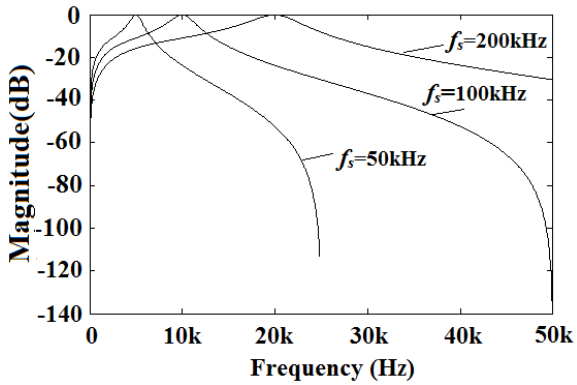


Fig. 10 Band-pass SI filter tuned by sampling frequency

3.3 Analysis of excess phase error

The SI filter structure based on single-ended FLF configuration has been investigated in [22], which requires current mirrors to produce signal inversion. It is well known that current mirrors would introduce excess phase errors. Thus, the sampling-to-cutoff frequency ratio should be larger in order to reduce the excess phase errors, which would introduce the magnitude distortion and nullify the advantages of bilinear z-transform. To overcome above shortcoming, this Letter proposes a fully-balanced SI filter structure based on FLF configuration, which can produce signal inversion simply by crossing over signal pairs.

To testify the advantage of fully-balanced structure over single-ended structure at reducing excess phase error, this Letter uses the low-pass filter in Section 3.1 as an example. Following the design procedure described in Section 3.1, one can determine the parameters in Fig.4 at sampling frequency of 50kHz: α_0=0.6, α_1=0.9, α_2=0.8, β_1=0.1101, β_2=0, β_3=0.2614, γ_1=0.7009, γ_2=0.9395, γ_3= 0.2614.

Fig.11 shows the realization circuits of (23) by using the single-ended FLF SI filter structure proposed in [22]. The parameters in Fig.11 at sampling frequency of 50kHz can be obtained as: α_1=0.7282, α_2=0.7282, α_{c1}=0.0661, α_{c3}=0.2130, α_{f1}=0.4205, α_{f2}= 0.6967, α_{f3}= 0.2130.

Fig.12 gives the magnitude frequency response of fully-balanced and single-ended third-order elliptic low-pass filter at sampling frequency of 50kHz. The magnitude response of single-ended filter has been distorted, in which the maximum value exceeds 0dB. It can be seen that the single-ended filter has higher magnitude distortion compared with fully-balanced filter along with the decrease of sampling frequency.

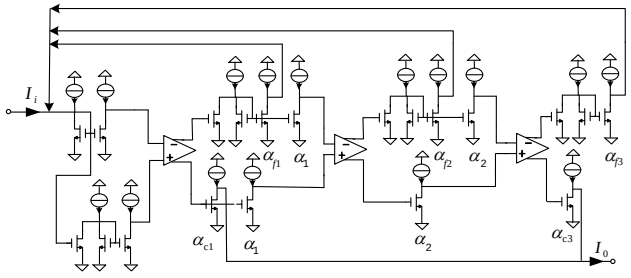


Fig. 11 Single-ended SI structure for low-pass filter

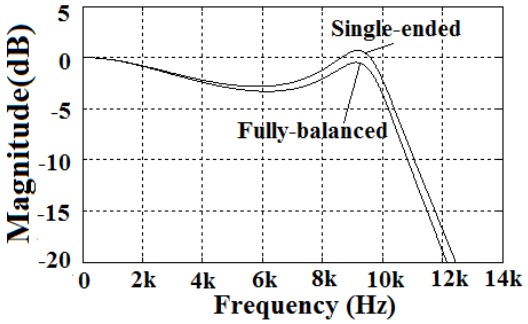


Fig. 12 Magnitude frequency response of fully-balanced and single-ended SI low-pass filter (f_s=50kHz)

4 Conclusions

The generation of double-sampling fully-balanced FLF SI filter structure has been presented. The proposed structure can realize arbitrary transfer function with low sensitivity, the feature that is particularly useful in the applications which require non-conventional zeroes such as biomedical and communication systems using wavelet transforms. Also, the proposed structure has simple synthesis method and explicit design formulas, which enables IC designers to synthesize high performance SI filters rapidly and accurately.

Acknowledgements

This work was supported by the Fundamental Research Funds for the Central Universities (grant 2012JBM006) and Specialized Research Fund for the Doctoral Program of Higher Education (grant 20130009120042).

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