A New SoC Video Ghost Canceller

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Abstract— **A video ghost canceller, which reduces the effect of multi-path signal echoes (ghosts), is described in this paper. An adaptive LMS algorithm was used to improve the received image quality of PAL or NTSC broadcasts. The internal 576-tap digital filter, which is comprised of a 144-tap FIR and a 430-tap IIR filter, cancels ghosts occurring from –6.15μS before to +41.6μS after the main signal. In order to reduce the chip area occupied by the filter, an algorithm that combines the error threshold and the error accumulation methods is applied for reducing the coefficients word-length. Also, a tap-decimated equalizer is proposed, which can greatly reduce the number of the multipliers in the adaptive filter. The system on chip (SoC) device performs all the functions required for ghost cancellation, eliminating the need for external DSP controllers, memory, sync detection, D/A converters, A/D converters, and user programming. From chip tests, the canceller can remove the ghost whose power is lower than –6dB compared to that of the main signal and make ghost residue down to -40 dB. When operating at a rate of 14.318 MHz (4Fsc), it dissipates 1.3W from a 3.3V power supply.**

Index Terms— **ghost canceller, adaptive LMS algorithm, digital filter, DSP**

I. INTRODUCTION

Broadcast television signals reflected from buildings, mountains, and other objects create time shifted and attenuated echoes (ghosts) of the originally transmitted signal. These imperfections strongly affect the perception of picture quality. So, effective ghost cancellation methodology is very important for improving television picture quality [1-3]. The ghost canceling filter is basically an inverse filter of the deghosting system. In order to cancel the ghosts, the filter coefficients have to be properly set. This is done by comparing the received ghost canceling reference (GCR) signal broadcast by the TV station with the standard GCR signal stored locally. Note that there are many attempts to implement ghost cancellers in the past twenty years [5-8]. However, they are very costly due to the use of high performance signal processors. Ghost cancellation systems have, therefore, never been popular.

The purpose of this paper is to propose a SoC ghost canceling device, which can complete all the functions required for ghost cancellation and is compatible with all GCR signal standards. All the DSP controllers, memory, sync detection, D/A converters, A/D converters and user programming are included in this ghost canceller IC, as shown in Fig.1.

The ghost cancellation algorithm and the adaptive equalizer design are discussed in Section II and Section III, respectively. Section IV explains the system implementation. The experimental results of the proposed video ghost canceller are summarized in Section V. Conclusions are given in Section VI.

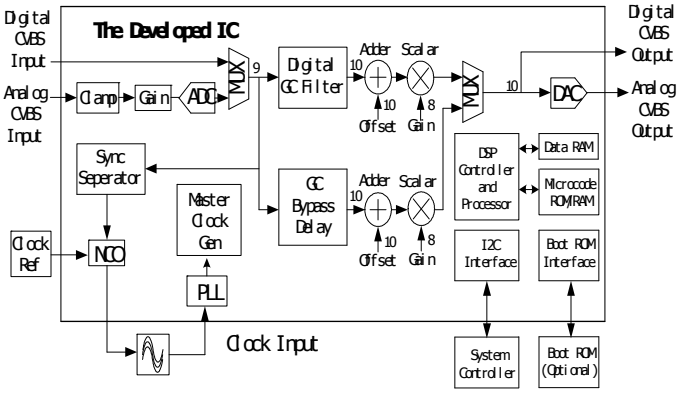

Fig.1 Deghosting system architecture

II. GHOST CANCELLATION ALGORITHM

The ghost cancellation algorithm is divided into three phases. In the first phase, the broadcast GCR is detected and sampled. The sampled GCR enables filter coefficient adaptation by the internal DSP unit in the second phase. Once the filter coefficients are calculated, cancellation is completed in the third phase by filtering the digitized video signal. The device includes custom algorithms for the detection and attenuation of ghosts using any international GCR standards.

Sampling and averaging of the broadcast GCR signal in the first phase of the algorithm eliminates the DC level and non-varying video signals that may be received, such as horizontal sync and color burst. After sampling and averaging, the broadcast GCR signal is correlated with the internally stored reference signal. The correction peak is examined for intensity to validate GCR presence in the received video signal. If the GCR is not present in the received video signal, the cancellation process is terminated and the video signal is digitally bypassed without processing. If a GCR is determined to be present, then the correlation output provides correction peaks for each echo, with the strongest peak of the correlation function equal to the main video signal.

In the second phase of the algorithm, a least mean square (LMS) algorithm, which has the advantage of stability and simplicity of hardware implementation, executes the calculation of the digital filter coefficients. An error vector is calculated by subtracting the internally stored reference GCR from the broadcast GCR. The error vector is then correlated with the filter input and the resulting

correction vector is used to adapt the filter coefficients in the algorithm's third phase.

The adaptation process is divided into Fast and Slow modes of operation. In Fast mode, a rapid adaptation of coefficients is executed after channel changed. This allows for a quick convergence of the filter and an immediate display of a corrected video image. A de-ghosted image is displayed in 1.7 to 11.2 seconds, depending on noise level. The algorithm then transits to Slow adaptation mode, tracking any changes in multi-path conditions. Filter performance is continually monitored to assure stability. If the filter should become unstable, the adaptation process is re-initialized and a new set of coefficients computed.

2.1 Optimization of the Word-Length for Filter Coefficients

In LMS, the weights of the filter that recovers the original signal are updated as follows,

$$C(t+1) = C(t) + \alpha e(t) Y(t) \quad (1)$$

$$e(t) = X(t) - Y(t) C(t) \quad (2)$$

where *C(t):* Coefficient vector, *Y(t):* Input vector, α: Convergence factor, *e(t):* Error signal and *X(t):* Desired signal. In order to reduce the chip area occupied by the multipliers in the adaptive filter, the error threshold and the error accumulation algorithms are applied for reducing the coefficients word-length. The error threshold method applies some threshold values to both the error and the input signal in order to neglect small changes, and only increases or decreases the filter coefficients value by 1. Note that multipliers are not needed for the coefficients adaptation. However, this method inevitably results in some performance loss. The error accumulation method equips a small extra register at each filter tap, and increases or decreases the value of the registers according to 'α **e*(*t*) **Y*(*t*)' When the value of the register overflows or underflows, it increases or decreases the value of the filter coefficients respectively. This method performs better than the original algorithm with multiplications because random adaptation effects are averaged out by accumulating the coefficients update signal before the actual adaptation. In this work, an algorithm that combines the error threshold and the error accumulation methods is used [2].

III. ADAPTIVE EQUALIZER DESIGN

3.1 Adaptive Equalizer Architecture

Ghost cancellation can be accomplished by passing a received signal through an equalization filter whose transfer function is the inverse of that of the channel. Exact inversion of the channel can be obtained by an infinite impulse response (IIR) equalizer while an approximate channel inverse can be achieved by a finite impulse response (FIR) equalizer. While an FIR equalizer requires more tapes than an IIR equalizer, an IIR equalizer is unstable for precursor ghosts, i.e., when the delayed signal is stronger than the original signal. In addition, an IIR filter has noise enhancement problems with close-in ghosts. For short ghosts, an FIR equalizer is usually sufficient. Here, a combination of FIR and IIR filters is used to reduce the number of taps required while ensuring stability for longer ghosts. The device's 576-tap internal digital filter, as shown in Fig.2, cancels ghosts occurring from –6.15μS before to +41.6μS after the main signal. The digital filter is comprised of a 144-tap FIR section whose first 88 taps reduce precursor ghosts and a 432-tap IIR section that eliminate post-cursor ghosts. The 432-tap IIR section is further divided into a 360-tap main filter block that eliminates all post-cursor ghosts occurring from 0 to +25μS after the main signal, and two 36-tap "floating" filter blocks that remove rare ghosts occurring from +25μS to +41.6μS after the main signal. The digital filter can remove the ghost whose power is lower than –6dB compared to that of the main signal and make ghost residue down to -40 dB.

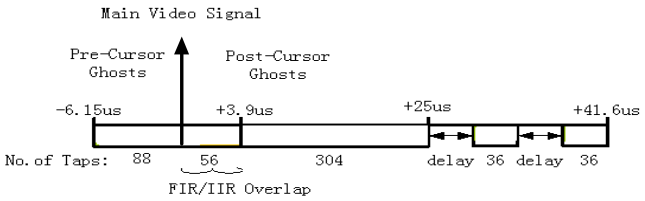

Fig.2 Deghosting filter structure

3.2 Optimization of the Equalizer

The most straightforward implementation for the FIR and IIR filters is to build the total number of taps required to deal with all echo situations. It would require many taps that could not be economically implemented. To solve this problem, this paper proposes tap-decimated equalizer which can greatly reduce the chip area occupied by the multipliers in the adaptive filter.

As we know, the filter coefficients for most of the taps in the conventional DFE would be zero, making the direct implementation very inefficient from the standpoint of hardware utilization. On the other hand, if each filter tap could be positioned independently in the time domain, the filter would require only one tap for each nonzero filter coefficient. Fig. 3 shows the diagram of the tap-decimated equalizer.

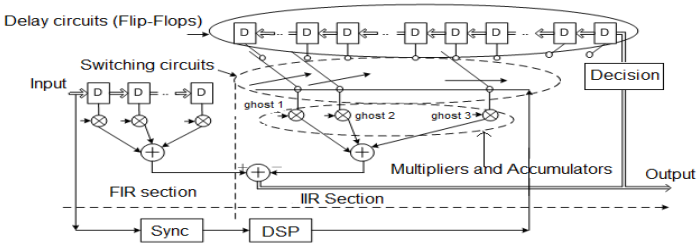

Fig.3 Tap-decimated equalizer diagram

The disadvantage of this approach is that a separate delay line would be required for each filter tap. An intermediate approach is to group a number of consecutive taps into sections, with a delay line for each section [4]. This yields reasonably effective use of the taps, since a single ghost requires many taps to cancel it. In this chip the decision was made to group the 576 taps into 8 filter sections, each with 72 consecutive taps. Each of these sections can be assigned to be part of the FIR filter or the IIR filter, and may be placed at an arbitrary temporal location by virtue of a dedicated programmable delay line output. To conserve filter sections and improve the signal-to-noise ratio, a separate unity-gain path was added to implement the main signal. The variable delay lines were implemented using dual port RAMs and appropriate control logic. Choice of the RAM and its exact configuration was based on minimization of area and power consumption.

IV. SYSTEM IMPLEMENTATION

4.1 Clamp, Input Gain, and A/D converter

The video input should be low-pass filtered to remove frequency components higher than the video bandwidth. The device features

an analog front end (AFE) with clamp circuit, programmable gain stage and internal 10-bit A/D converter.

The clamp position is code programmable. The position can be set anywhere along either the sync tip or the back porch. Nominally, the two clamp voltages are set by analog input pins. Through microcode, one of the two clamp reference levels is selected for normal operation. Also with the code, the relative position and duration of the clamp at the selected reference level is set. The gain block prior to the A/D controls the amplitude of the input video signal. Through code control nominal dynamic range is maintained.

The A/D converter consists of two parts: a pipelined analog front end and a digital back end for correcting and calibrating pipe stage results for parallel output. It works in the classical pipelined fashion. After the sample and hold circuitry, each successive stage approximates the error between a specific bit's analog equivalent and the propagated error result from the previous stage. Digital results from each stage are grossly corrected to coincide in time with the results from the preceding stages. A latency of 9 clocks is required before the sampled input is completely converted and the digital output available. The A/D's noise floor is better than 59dB at Nyquist sampling frequencies below 25MHz and has a THD of better than 60 dB.

4.2 Digital to Analog Converter (DAC) [9]

The device features a 10-bit, 200MHz digital to analog converter (DAC). This DAC is based on the segmented architecture, as shown in Fig. 4, where the DAC is composed of a unit decoded matrix for 6 MSB's and a binary weighted array for 4 LSB's. A new switching scheme is employed to reduce INL errors due to current mismatch in the unit decoded matrix for 6 MSB's.

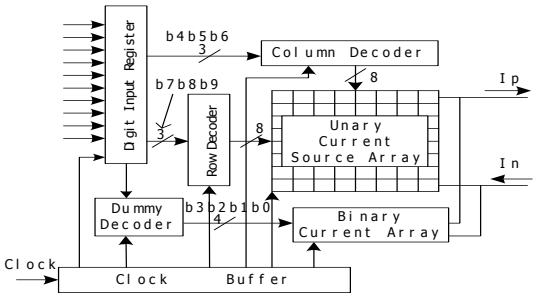

Fig.4 Block diagram of the proposed DAC

In the unit decoded matrix, it is difficult to make current sources identical due to layout mismatches, thermal distribution differences inside a chip, voltage drops along power supply lines, and process deviations. The nonlinear secondary effects cause graded, symmetrical, and random errors, resulting in the reduced linearity of DAC's [10-11]. The proposed DAC employs a new switching scheme to minimize the degradation of integral linearity caused by mismatches of current sources. As shown in Figs. 5 and 6, the proposed switching scheme can reduce two-dimensional graded and symmetrical errors more efficiently. The simulated integral nonlinearity (INL) characteristics of three conventional switching schemes (a), (b), (c) and the proposed switching scheme (d) are illustrated and compared in Fig. 6, assuming graded and symmetrical errors of 2%, respectively. It is noted that the proposed switching scheme shows the best INL characteristic. According to measurements, SFDR of over 55dB is achieved. When operating at 200M Sample/s, it dissipates 82 mW from a 3.3 V power supply. The measured DNL and INL are 0.3 LSB and 0.2 LSB, respectively. The device not only offers differential analog outputs, but also a 10-bit digit output. The digital output is maintained in order to provide a seamless handshake to digital video processing circuits that it drives.

62	58	54	50	49	53	57	61	31	27	23	19	20	24	28	32
46	42	38	34	33	37	41	45	15	11	7	3	4	8	12	16
14	10	6	2	1	5	9	13	47	43	39	35	36	41	44	48
30	26	22	18	17	21	25	29	63	59	55	51	52	56	60	64

Fig.5 Proposed switching sequence for the 6 bits unit decoded matrix

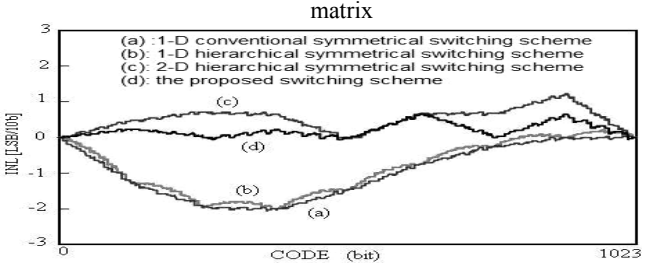

Fig.6 Simulated INL characteristic based on switching schemes

After the ghost cancellation circuitry are programmable offset and gain blocks. The ghost-cancelled signal loses its clamp level and gain during processing. The offset and gain blocks serve to digitally set the clamp level and signal gain, satisfying the requirements of ensuing circuitry. In this way, the digital output has well defined characteristics and does not need to be clamped and converted for a second time.

4.3 Input Reference Clock and PLL

DSP-based signal processing devices require a synchronized time base, a master clock that is synchronized to the received signal. In Slaved mode, this clock is externally generated by a master device such as 3D Y/C separator (comb filter) and is fed via the clock_in pin. In Stand Alone mode, the master clock is internally generated. To generate the synchronized time base, this device use an internal numerically controlled oscillator (NCO) that is operated by the internal DSP processor. A block diagram of the NCO-base clock synthesizer is shown in Fig.7. It can also accept an externally generated sample clock.

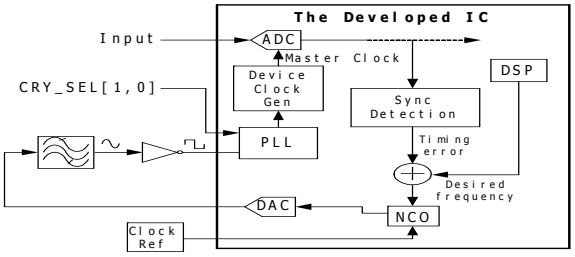

Fig.7 NCO block diagram

In operation, the NCO outputs digital samples of a sine wave that is stored in the internal look-up table. The data is output at a fixed frequency determined by the external reference clock. The frequency of the output sine wave, lower than the sample rate (below Nyquist), is determined by the values stored in the look-up table. The internal DSP processor controls the stored values. The NCO output is fed through the internal DAC to produce an analog sine wave. To generate a digital clock signal equivalent to the analog sine wave frequency, the DAC output is low-pass filtered and then passed through a squaring circuit. The low-pass filter provides smoothing of the DAC output, removing the quantization levels of the DAC outputs. The squaring circuit consists of an

inverter, which is being used as a comparator. The advantage of the NCO-based timing circuit is that an arbitrary clock frequency, within a certain frequency range, can be generated from another reference frequency. For this device, acceptable frequency inputs are between 10 MHz and 75 MHz (tolerance of +/-200ppm is allowed). By using a DAC to generate sine wave samples, a low-pass filter can be used to construct the entire waveform, and the zero crossing point is detected with a simple inverter circuit resulting in a periodical clock with clock edges that are not coincident with the NCO reference clock. The DSP compares the synthesized master clock to the timing parameters within the received signal, and adjusts the NCO to maintain synchronization. Several multiplication factors for the internal PLL are used. Selection of the multiplication factor is done using the CRY_SEL[1,0] input pins. This results in internal master clock with frequency equal to the product of the multiplication factor and the CLOCK_IN frequency. The D_STRB output operates in this frequency.

V. EXPERIMENTAL RESULTS

Fig. 8 shows DAC's static characteristics by single-ended measurements. The maximum DNL and INL are +0.20/-0.30 LSB and +0.20/-0.19 LSB, respectively. This clearly shows the advantage of the switching sequence.

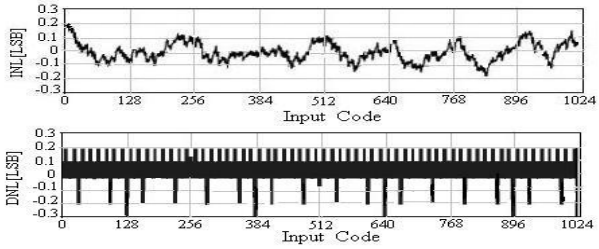

Fig.8 Static characteristics of the DAC

The proposed video ghost cancellation IC including DSP controllers, memory, sync detection, D/A converters, A/D converters, and user programming, as shown in Fig.9, was fabricated in 0.35um CMOS. When operating at a rate of 14.318 MHz (4Fsc), it dissipates 1.3W from a 3.3V power supply. A summary of the key performance characteristics is given in Table 1. Comparison with other ghost cancellers is presented in Table 2.

VI. CONCLUSIONS

In this paper, a video-rate adaptive equalizer IC that reduces the effect of multi-path signal echoes (ghosts) is described. The internal 576-tap digital filter cancels ghosts occurring from –6.15μS before to +41.6μS after the main signal. An algorithm that combines the error threshold and the error accumulation methods is used for optimization of the word-length for filter coefficients. In order to reduce the chip area occupied by the multipliers in the adaptive filter, a tap-decimated equalizer is proposed. From chip tests, the canceller can remove the ghost whose power is lower than –6dB compared to that of the main signal and make ghost residue down to -40 dB. The device was encapsulated in 80-pin plastic QFP package with an active area of 280 mm2. When operating at a rate of 14.318 MHz (4Fsc), it dissipates 1.3W from a 3.3V power supply.

VII. REFERENCES

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Table 1 Typical performance characteristics (25^0C)

Technology	0.35 μm CMOS
Die Size	280 mm^2
Number of Taps in Adaptive Equalizer	576
Input Resolution	10 bits
Algorithm used for Updating Coefficients	LMS
Operating frequency	14.32 MHz@3.3V supply
Internal World Length	18 bits
Number of Bits in the Multipliers	10 bits by 8 bits
Total Power Dissipation	1.3W@ 3.3 V

Table 2 Comparison with other ghost cancellers

Design	Edwards [4]	Pao [7]	This work
Input Resolution	8 bits	10 bits	10 bits
Number of taps	180	64	576
Technology	1.0μm CMOS	0.8μm CMOS	0.35μm CMOS
Power consumption	2.5W @14.32 MHz	2.3W@18 MHz	1.3W@14.32 MHz
Die area	56.25mm^2	12.6 mm^2	280 mm^2

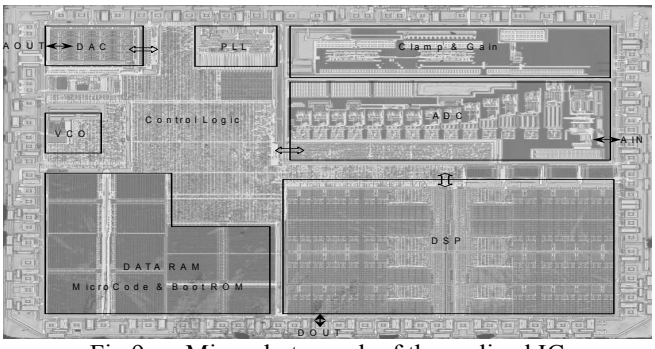

Fig.9 Microphotograph of the realized IC