Real-Time Digital Video Multiplexer Synchronisation Implementation with CPLD

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Abstract

Many video applications in security areas such as close circuit television (CCTV) require multiple video channels which must be multiplexed into a single video stream. The industry can only afford to have a few frames or fields per camera. This paper emphasises on a novel hardware design using an algorithm for synchronising the analogue video inputs. Therefore the proposed multiplexer system is able to achieve a constant stream of 50 digital video fields per second using a CPLD (Complex Programmable Logic Device) for 625/50 video system.

Background

The composite analogue inputs are converted to 8bit ITU-R (International Telecommunication Union – Radiocommunication) BT.656 format data. This international standard defines the encoding parameters of digital television [1]. The important feature of this digital format is its PAL (Phase Alternative Line) / NTSC (National Television Standard Committee) compatibility. Hence, the active video resolution is either 720 × 288 per video field for PAL standard or 720 × 243 for NTSC standard. The YCbCr signal of ITU-R 601 is multiplexed producing the parallel digital signal sampled at 27MHz frequency. This digital format is also widely used in most video surveillance applications because it offers a high video definition and the synchronisation signals are embedded into it. This makes it easier to be interfaced with other peripherals.

The fundamental of the multiplexing algorithm is time division multiplexing (TDM). TDM is a multiplexing technique where each video field is assigned to a time interval and takes turns in sequence.

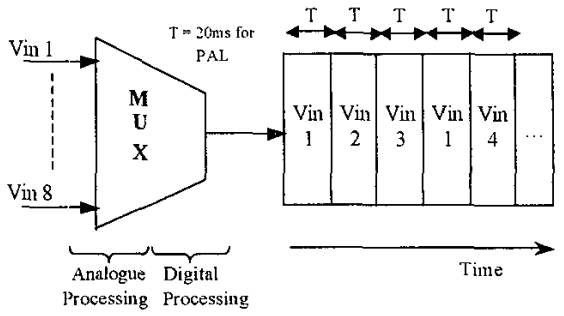

Figure 1: TDM applied for video multiplexer

Features

Functions of the real-time multiplexer include a camera priority selection predefined by the user. For example, in an 8-camera input system as shown Figure 1, for video input 1 (Vin1), the operator requests 15 fields per second in the output stream over the 50 available. The other seven camera inputs have an equal priority and share the remaining 35 fields. The video field output is sequenced as shown in Table 1. In this sequence, the video fields of each camera are customarily distributed.

The video output stream can then be compressed into an MPEG (Motion Picture Experts Group) format [2-4] or into a Wavelet compressed format [5]. Furthermore, the compressed video can be transferred to a computer and stored into its hard-disk. The playback can therefore be achieved on the monitor. The analogue video inputs are interlaced. In order to reduce the flicker effect while playing back the video, a single parity field is processed. Only the odd parity fields are on the digital output stream in this application.

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Table 1: Generated Field sequence according to the priority of each camera.

Field number	1	2	3	4	5	6	8	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Camera source	2	1	3	2	4	5	2	6	7	2	8	1	2	3	4	2	5	6	2	7	8	2	1	3	2

Field number	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Camera source	4	5	2	6	7	2	8	1	2	3	4	2	5	6	2	7	8	2	1	3	4	5	6	7	8

Description of the system

The block diagram of the real-time digital multiplexer is shown in Figure 2. The multiplexing system can input an unlimited number of video inputs. Only 8 video sources are taken into consideration in this paper. Vin 1~8 are analogue composite signals from video cameras. The analogue video matrix feeds the analogue sources to the Video Processor Blocks in the paths 1, 2 and 3. The Video Processor Block are the video analogue to digital converters, which generate a continuous digital stream from a particular camera in the ITU-R BT.656 format [6]. In their respective paths, the Video Field Blocks contain First In First Out (FIFO) memories with a storage capacity for one video field. The CPLD behaves as a FIFO controller and is implemented in a Lattice ispLSI 1048EA [7]. The CPLD controls the write sequence for each path and the full read sequence. Also, the controller takes into account the camera field sequence provided by a microcontroller as shown in Table 1. A synchronisation signal capture mechanism is adopted in order to capture the vertical synchronisation (Vsync) from the desired cameras. This way, a full 8-bit digital video stream is produced without any time gap between two fields.

State-machine

The principal problem is that all video inputs are from different cameras. However the cameras are not synchronised among themselves, in other words a genlock signal is not utilised. In order to generate the digital stream without any time gap between the fields, a strict synchronising mechanism must be accomplished. Therefore, a state-machine in CPLD is implemented to switch smoothly the digital video fields into a single stream. The state-machine is illustrated in Figure 3.

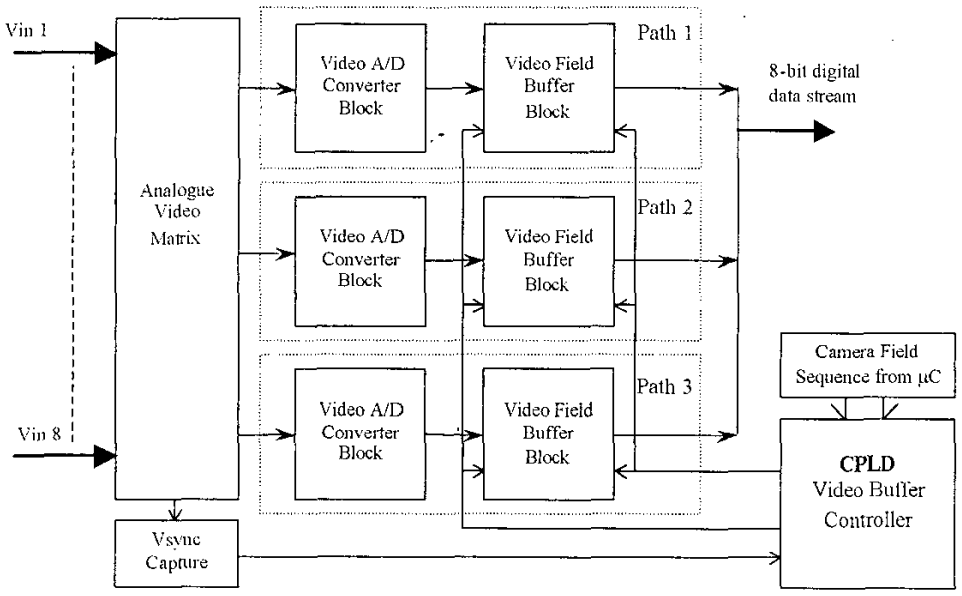

Figure 2: Block diagram of the real-time digital multiplexer

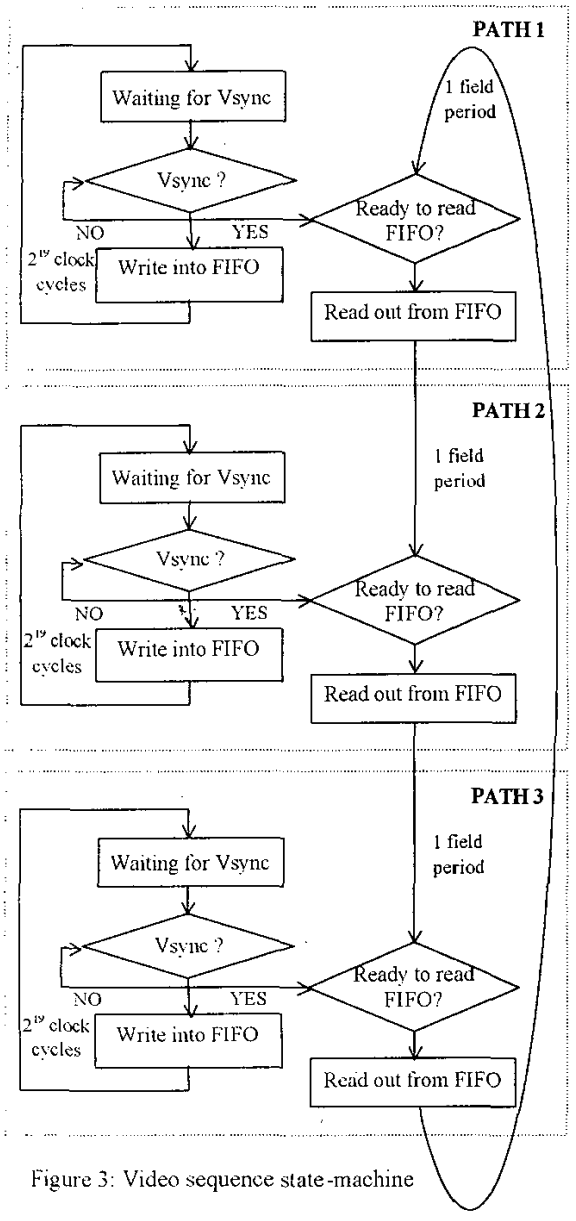

Figure 3: Video sequence state-machine

The video matrix switches the video inputs according to the pre-generated sequence (shown in Table 1). For the 3 video paths, all the video data is fed asynchronously into the video field memories after digital conversion. The first stage is to capture the Vsync, which initiates the start of a write sequence from any of the path.

Once Vsync in path 1 has been received by the CPLD, the FIFO controller authorises the start of write sequence as well as the start of read sequence for the video FIFOs. In parallel, the Vsyncs from paths 2 and 3 are waiting to be caught. When they are received, their FIFO write sequence starts in their corresponding paths.

When a video field has been fully stored into the video buffer, the Vsync is re-activated for the next camera of the stream sequence.

Once the first three digital fields have been read out from the video buffers, then the path 1 FIFO memories are ready to be read out. Hence, the read sequence loop is continuously repeated.

Figure 4 depicts the synchronisation timings between the paths. A Vsync of any video input appears within a two-field period, which is represented by $T1_X$ in figure 5 with X the field number in the sequence. $T2_X$ stands for the duration where a FIFO write sequence may be active.

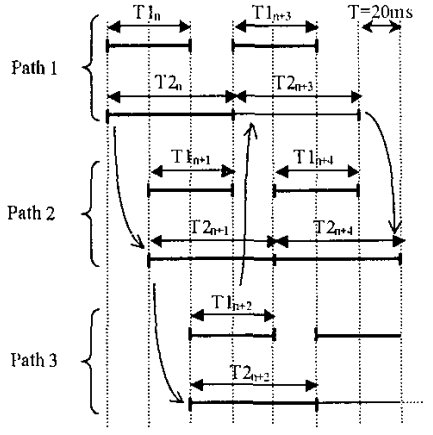

Figure 4: Sketch of synchronisation timings

The FIFO read sequence is achieved as follows TX_n, TX_{n+1}, TX_{n+2}, TX_{n+3} and so on. According to the randomness of the occurrence of a Vsync capture of the desired single-parity field, it can be stated that the time allocated to write a complete field takes three field periods in the worst case. It is also noticed that there is one field period between the start of Vsync capture interval between two consecutive paths. Consequently, it is proven that three video paths are required to achieve the whole multiplexer algorithm.

Results

A test board has been built based on the block diagram shown in Figure 2. After having debugged the hardware and the software, the video output stream was visualised by converting back to an analogue signal. The video inputs connected to the board are not synchronised. Figure 5 demonstrates the synchronisation algorithm by generating the 50 fields per second video sequence in 625/50 video system.

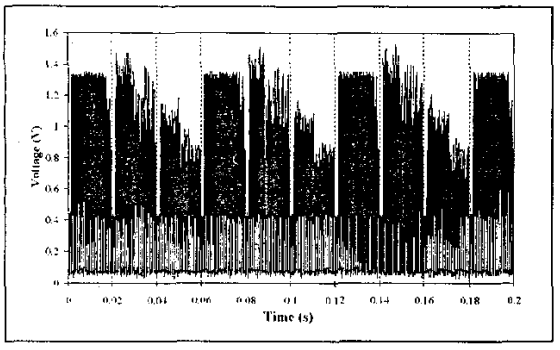

Figure 5: Video output stream back to analogue

Conclusion

A real-time digital video multiplexer has been implemented with a CPLD. It has been shown that the requirements to achieve a digital video stream without time loss between two fields were met. The specific features of this multiplexer system are that the cameras are not synchronised and single-parity fields are processed in order to improve the quality of the display during playback. The application of CPLD significantly improves the precise video timing controls and also reduces design complications and implementation time.

The number of video inputs can be increased indefinitely by cascading analogue matrices. This can be done without modifying the synchronisation algorithm. Furthermore, it only requires minor timing re-configurations to adapt the compatibility of the same hardware design for a 525/60 video system.

References

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