A 12-bit 150-MHz 1.25-mm^2 CMOS DAC

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ABSTRACT

This paper presents a 12-bit 150-MHz current steering DAC with hierarchical symmetrical switching sequence that compensates gradient errors. The circuit of the DAC employs segmented architecture; the least significant bits (LSBs) steer a binary weighted array, while the most significant bits (MSBs) are thermometer decoded and steer a unary array. The measured differential nonlinearity and integral nonlinearity are $\pm$ 0.6 LSB and $\pm$ 0.9 LSB, respectively. The circuit is fabricated in 0.5 μm, two-poly two-metal, 5.0V, mixed-signal CMOS process. It occupies $1.27mm \times 0.96mm$ chip area, when operating at 150 MHz and dissipates 91.6mW from a 5.0V power supply, which is much smaller than that of [1].

1. INTRODUCTION

In recent years, research of high-speed and high-resolution digital-to-analog converters (DACs) has attracted much attention [1-22] and such DACs have been widely applied in communication and information systems, for example, asymmetrical digital subscriber loops (ADSL), GSM baseband I/O port integrated circuits, high-resolution displays for computer graphics and high-definition television (HDTV). With the ability to integrate analog circuits with memory and digital signal processing (DSP) circuits on the same die, CMOS technology is preferred for modern SOC design. The CMOS DAC has advantage of low power, low cost, and I/O compatibility with both TTL and external CMOS circuits. To achieve both high resolution and high speed as required in many communications and display systems are a major design challenge for CMOS DACs due to various factors. Generally, CMOS DACs have a low conversion rate, or, if the speed is satisfactory, a high power consumption.

Linearity can be achieved by overcoming all possible random and systematic errors [7]. The random errors are determined by the inherent matching properties of the technology used. In a given process technology, for architectures that do not incorporate trimming or tuning, increasing the active area of each unit element in the arrays of DACs is the most effective method for reducing random errors. Optimizing switching schemes can reduce the nonlinearity due to gradient errors. This potential has been seen in many current-steering DAC designs [8, 9]. A switching scheme is actually a layout technique. In a current-steering DAC, the switching scheme determines the interconnection between the outputs of the

thermometer decoder/latch and the control terminals of switches in the current matrix.

Among several CMOS DACs proposed so far, some have a low conversion rate [10-12], while others have large power consumption [12]. This paper describes a 12-bit 150MHz CMOS current steering DAC with low power consumption. It was fabricated in 0.5 μm, two-poly two metal, mixed-signal CMOS process and occupies $1.27mm \times 0.96mm$ chip area. This current steering DAC is based on the current cell matrix design [13] and can drive a load resistor without an output buffer. The hierarchical symmetrical switching sequences suppress gradient errors, symmetrical errors, and random errors distributed throughout the outputs of current cells.

2. BASIC CONFIGURATION

Fig.1 shows the architecture of the 12-bit CMOS current steering DAC, where the least significant bits (LSBs) steer a binary weighted array, while the most significant bits (MSBs) are thermometer decoded and steer a unary array. The 12-bit DAC employs segmented architecture of "8+4" whose output currents are summed up with the outputs of the thermometer-decoded DAC and binary weighted DAC. The MSBs contain 256 current sources that are ideally identical. The switching scheme determines the order the current sources are switched on as the digital code increases from 1 to 255. The LSBs are composed of a 4-bit binary-weighed DAC.

To design a high-resolution 12-bit DAC, if all current cells employ the thermometer decoded architecture, $2^{12} = 4096$ unit current sources will be required. Each unit current source is connected to a switch controlled by the signal coming from the binary-to-thermometer decoder. When the digital input increases by 1 LSB, one current source is switched from the negative to the positive side. Assuming positive-only current sources, the analog output is always increasing as the digital input increases. In addition, there are several other advantages for a thermometer decoded DAC compared to its binary-weighed counterpart. First, the matching requirement is much relaxed, 50% matching of the unit current sources is good enough for DNL< 0.5 LSB. At the mid-code, a 1 LSB transition (0 111 111 111 – 1 000 000 000) causes only one current source to switch as the digital input increases by one only. This greatly reduces the glitch problem. Compared with the binary weighed DAC, one major drawback of the thermometer decoded DAC is the chip area, since for every LSB, this architecture needs a current source, a switch, and a decoding circuit, as well as the binary to thermometer decoder.
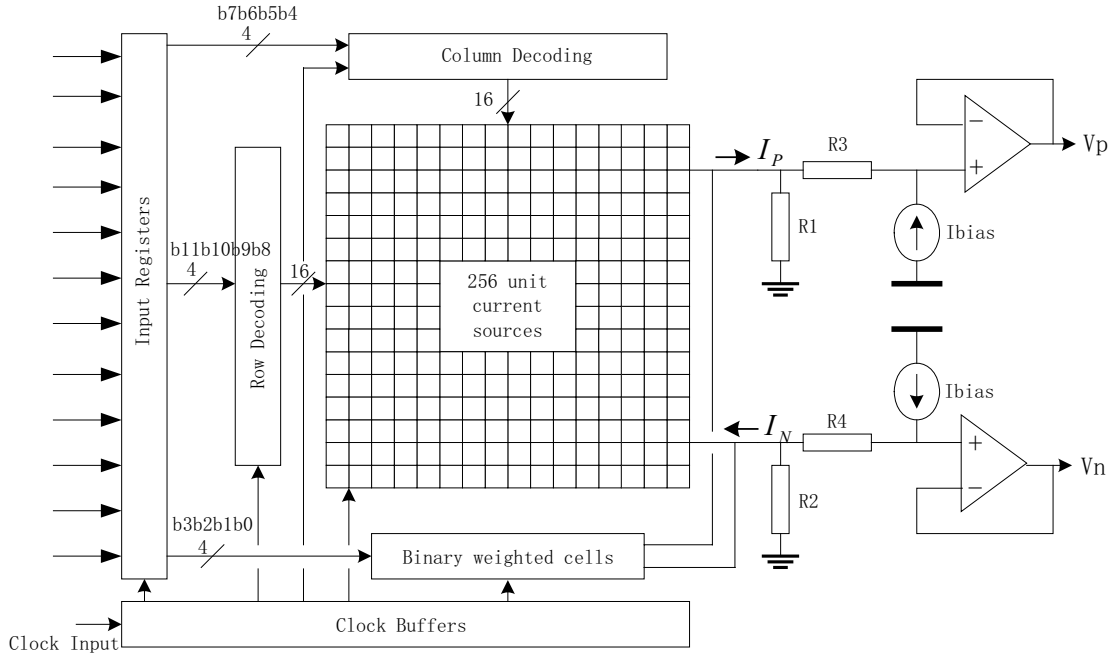
Fig.1.   Basic configuration of the DAC

3. HIERARCHICAL SYMMETRICAL SWITCHING

In the current cell matrix configuration, the outputs of current cells must be identical. However, the actual outputs of these current cells are not identical due to the following reasons:

   (1) A voltage drop along power supply lines can cause a symmetrical error.
   (2) Thermal distribution inside the chip can cause a symmetrical error.
   (3) There can be other types of errors such as a random error.

The final error distribution in the current cell matrix is given by the sum of all these errors. The errors of conventional symmetrical switching generally contain two parts; the first part is graded errors and the second is symmetrical errors. The conventional symmetrical switching has the advantage of compensating the graded errors of current sources [17]. In this switching sequence, current sources located symmetrically about the center are turned on. Then, a graded error caused by a certain current source is canceled by the current source located symmetrically. On the other hand, if current cells have errors distributed symmetrically, the conventional symmetrical switching cannot cancel them. To cancel multiple types of error, a switching sequence called the "hierarchical symmetrical switching" has been developed.

For hierarchical symmetrical switching, both graded and symmetrical errors are suppressed.

When the digital input increases, the component of graded error caused by a pair of current sources is canceled by the pair selected successively, while the component of symmetrical error caused by a current source is canceled by the current source selected successively.

Errors of conventional symmetrical switching can be defined as follows:

$$\varepsilon_G(k) = \frac{2k - N - 1}{2(N-1)} \times \varepsilon$$

$$\varepsilon_S(k) = \frac{N/2 - (2k - N - 1)}{N-2} \times \varepsilon \qquad (1)$$

where $\varepsilon_G(k)$ and $\varepsilon_S(k)$ are the graded error and symmetrical error of the k-th current source which corresponds with the k-th switching. Assuming the number of current sources N is a multiple of 4, the integral linearity error caused by the graded errors, INL_G and the integral linearity error caused by the symmetrical errors, INL_S are given as follows.

（1）Conventional symmetrical switching：

$$INL_G = |\varepsilon_G(1)| \; , \; INL_S = \left| \sum_{k=N/4+1}^{3N/4} \varepsilon_S(k) \right| \qquad (2)$$

（2）Hierarchical symmetrical switching：

$$INL_G = |\varepsilon_G(1) + \varepsilon_G(N/2)|$$
$$INL_S = |\varepsilon_S(1)| \qquad\qquad (3)$$

From (2) and (3), we can see that a linearity error in the conventional symmetrical switching caused by the symmetrical errors is proportional to N. On the other hand, in the hierarchical symmetrical switching, accumulation of its linearity errors is avoided since errors caused by current sources in every cycle can be compensated.

In an n-bit thermometer decoded DAC, the number of unit current sources that are ideally identical is N ($N = 2^n$). However, mismatches between the current sources always exist. For example, in a current-steering DAC, the actual current provided by current source j ($1 \leq j \leq N$) can be expressed as:

$$I_j = \bar{I}(1 + \varepsilon_j) \qquad (4)$$

where $\bar{I}$ is the average current provided by all the current sources in the array and ε_j is the relative deviation of I_j from $\bar{I}$. Hence:

$$\bar{I} = \frac{\sum_{j=1}^{N} I_j}{N} \quad , \quad I_{LSB} = \frac{I(N) - I(0)}{N} \qquad (5)$$

where I_{LSB} is the current step corresponding to that of 1 LSB.

In the design of a n-bit DAC, there are N unit current sources, including a dummy current cell. When the input digital number is K ($0 \leq K \leq N - 1$), the value of INL and DNL (differential linearity error) are as follows:

$$INL(K) = \frac{I(K) - I(0)}{I(N-1) - I(0)} \times (N-1) - K$$

(6)

$$DNL(K) = \frac{I(K) - I(K-1)}{I(N-1) - I(0)} \times (N-1) - 1$$

(7)

when the input digital number is K, the actual output current can be expressed as:

$$I(K) = \sum_{j=1}^{K} I_j + I(0) \qquad (8)$$

From the above, when the input digital number is K, INL(K) and DNL(K) are as follows, when the array of current sources include a dummy current cell.

$$INL(K) = \frac{\sum_{j=1}^{K} \varepsilon_j + \frac{K}{N-1} \varepsilon_N}{1 - \frac{\varepsilon_N}{N-1}} \approx \sum_{j=1}^{K} \varepsilon_j \qquad (9)$$

$$DNL(K) = \frac{\varepsilon_K + \frac{\varepsilon_N}{N-1}}{1 - \frac{\varepsilon_N}{N-1}} \approx \varepsilon_K \qquad (10)$$

The INL and DNL of an n-bit DAC can be expressed as:

$$INL_{DAC} = \max_{K=1}^{N-1}(|INL(K)|) \qquad (11)$$

$$DNL_{DAC} = \max_{K=1}^{N-1}(|DNL(K)|) \qquad (12)$$

From [9-12], it is apparent that thermometer decoded DACs can achieve very low DNL_{DAC}. For each element in the array, 50% matching is good enough to obtain one DNL_{DAC} of 0.5 LSB. However, it can be shown that with a poor switching sequence, the INL_{DAC} can be very high when gradient errors are present. Our goal is to minimize INL_{DAC} by optimizing the switching sequence.

4. MEASUREMENT and SIMULATION RESULTS

The 12-bit current steering DAC has been simulated and fabricated. The technology used is a 0.5 μm, two-poly two-metal, 5.0V, mixed-signal CMOS process of Taiwan UMC. The active area of the DAC is $1.27mm \times 0.96mm$. When operating at 150-MHz, it dissipates 91.6mW from a 5.0V power supply. Both measurement and simulation results show that the differential nonlinearity and integral nonlinearity are $\pm$ 0.6 LSB and $\pm$ 0.9 LSB, respectively. Measurement results of the chip are shown in Table 1.

The INL simulation result of the 12-bit DAC is shown in Fig.2. When operating at 150-MSample/s, the frequency of the input signal is 20MHz, 1 LSB=0.6mV, integral nonlinearity of DAC is lower than $\pm$ 0.9 LSB .Fig.3. shows the simulation result of DAC transient response, from which rise and fall times can be determined as 0.7ns.

5. CONCLUSIONS

A 12-bit 150-MHz current steering DAC based on a current cell matrix has been developed. A hierarchical symmetrical switching sequence has been introduced. This switching sequence suppresses both graded and symmetrical errors distributed in the outputs of current cells. A layout technique that reduces the differential linearity error is adopted. A current source cell with latch has been used to achieve high-speed performance. The DAC has been fabricated using 0.5 μm, two-poly two-metal, mixed-signal CMOS technology. When operating at a single power supply of 5.0V, the DAC dissipates 91.6mW at 150-MHz clock rate. The active area of the DAC is $1.25mm^2$, which is much smaller than that of [1], $3.2mm^2$
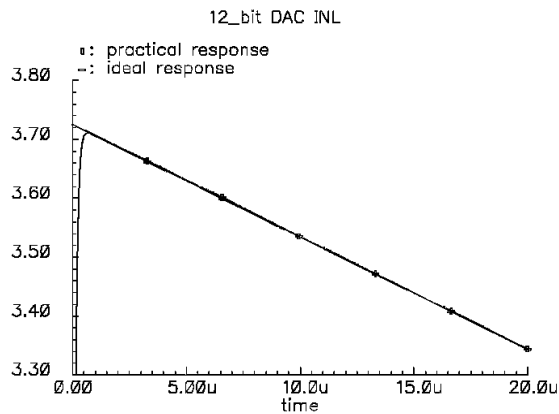
Fig.2   Integral Nonlinearity (INL) of 12-bit DAC

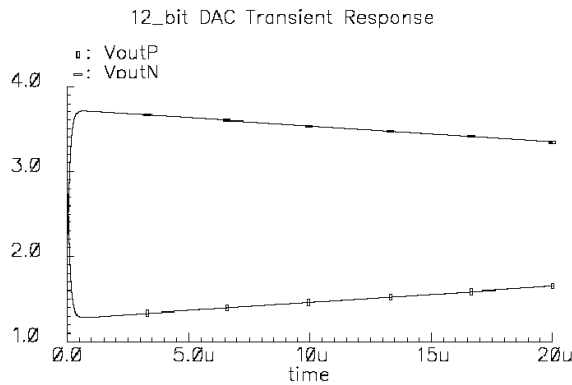

Fig.3.   Transient response of 12-bit current steering DAC

Table 1   Measured results of 12-bit current steering DAC

Technology	0.5 μm, 2P2M (UMC), mixed-signal CMOS
Resolution	12-bit
Differential Nonlinearity （DNL）	$\leq \pm 0.6$LSB
Integral Nonlinearity (INL）	$\leq \pm 0.9$LSB
Sampling Frequency	150-MHz
Output Swing	$2.5 V_{P-P}$
Rise/Fall Time （10% ~ 90%）	0.7ns
Power Dissipation （150MSample/s）	91.6mW
Power Supply	5.0V
Chip Area (one DAC)	$1.27mm \times 0.96mm$

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